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COMPLEX

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First Report on Preparation of Training Material and Organization and Execution of Courses/Workshops

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History of Changes

ED.	REV.	DATE	PAGES	REASON FOR CHANGES
KG	1.0	2011-12-01	8	Initial version
AM	1.1	2012-05-12	29	Integrated input of all contributing partners

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1 Introduction

This document is intended to present COMPLEX activities focused on education and training. In the first part of the project overall activities on education in a broad sense, encompassing mainly dedicated workshops and conferences, were undertaken by the consortium, more focused training courses will be prepared by partners in the second part of the project in the addition to the planned conferences and workshops.

2 Conferences

2.1 DATE 2011 – Design Automation and Test in Europe

During the 23rd European SystemC Users' Group Meeting (ESCUG), co-located with DATE'2011 in Grenoble, a practical introduction to the new `sc_vector` addition in the recently released updated SystemC standard IEEE 1666-2011 has been given. This new feature greatly improves the capabilities of SystemC to model regular structures and can increase modeling productivity.

sc_vector<T> Container and the IEEE P1666-2011 SystemC Standard

Philipp A. Hartmann, OFFIS

Abstract: In many designs, a parametrisable number of modules, channels, ports, or other SystemC objects are used. Since such SystemC objects are usually named entities in the hierarchy, it is either required (in case of modules), or at least desired to pass a name parameter to the constructor of such objects. In this talk, an introduction to the convenience container called `sc_vector<T>` for collections of such objects is given, which will be part of the upcoming IEEE P1666-2011 SystemC standard to lift this burden.

2.2 FDL 2011 – Forum on specification & Design Languages

The FDL2011 conference was organised by ECSI in Oldenburg, Germany, September 13-15, 2011. A complete program is presented at www.ecsi.org/fdl2011.

COMPLEX Project presented several related papers at the conference:

Session UMES2, Wednesday, September 14, 16:00-17:30

A Framework for the Generation from UML/MARTE Models of IP-XACT HW Platform Descriptions for Multi-Level Performance

Fernando Herrera and Eugenio Villar (University of Cantabria)

Session LBSD2, Wednesday, September 14, 16:00-17:30

Impact Simulation of Changes to Development Processes: An ESL Case Study

Frank Poppen, Roland Koppe, Axel Hahn and Kim Grüttner

Session LBSD3, Thursday, September 15, 11:00-12:30

SystemC Refinement of Abstract Adaptive Processes for Implementation into Dynamically Reconfigurable Hardware

Fernando Herrera, Eugenio Villar and Philipp A. Hartmann

ESCUG Meeting, Tuesday, September 13, 16:00- 18:30

Non-intrusive TLM-2.0 Transaction Observation, Interception, and Augmentation

Philipp A. Hartmann, Maher A. Fakih and Kim Grüttner

A special page has been devoted to COMPLEX in the FDL2011 Final Program to announce all the activities related to the project at the conference:

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**The 2011 Forum
on Specification
& Design Languages
Program**


**Oldenburg, Germany
September 13th-15th, 2011**

General Chair:
Frank Oppenheimer
 OFFIS, Germany

FDL is an  event |

COMPLEX Project at FDL 2011



The COMPLEX (COdesign and power Management in PPlatform-based design space EXploration) consortium develops a new design environment for platform-based design-space exploration offering developers of next-generation mobile embedded systems a highly efficient design methodology and tool chain. The integrated environment allows iterative exploration and refinement of advanced applications to meet market requirements. The design technology in particular enables fast simulation and explores the use of different implementations at Electronic System Level (ESL) with up to bus-cycle accuracy at the earliest instant in the design cycle. The main objectives are:

- Highly efficient and productive design methodology and holistic framework for design space exploration of embedded HW/SW systems.
- Combination and augmentation of well-established ESL synthesis & analysis tools into a seamless design flow enabling performance & power aware virtual prototyping of the HW/SW system.
- Interfacing next-generation model-driven SW design approach and industry standard model-based design environments.
- Multi-objective co-exploration for assessing design quality and optimizing the system platform with respect to performance, power, and reliability metrics.
- Fast simulation and assessment of the platform at ESL with up to bus-cycle accuracy at the earliest instant in the design cycle.
- Optimization benefits from run-time mode adaptation techniques, such as dynamic power management or application adaptation to varying workloads.

COMPLEX related papers presented at FDL 2011:

Session LMS32, Wednesday, September 14, 16:00-17:30
 A Framework for the Generation from UML/MARTE Models of IP-XACT HW Platform Descriptions for Multi-Level Performance
 Fernando Herrera and Eugenio Villar (University of Cantabria)

Session LBS02, Wednesday, September 14, 16:00-17:30
 Impact Simulation of Changes to Development Processes: An ESL Case Study
 Frank Poppen, Roland Köppe, Axel Hahn and Kim Grütner

Session LBS03, Thursday, September 15, 11:00-12:30
 SystemC Refinement of Abstract Adaptive Processes for Implementation into Dynamically Reconfigurable Hardware
 Fernando Herrera, Eugenio Villar and Philipp A. Hartmann

ESCUG Meeting, Tuesday, September 13, 16:00-18:30
 Non-Intrusive TLM-2.0 Transaction Observation, Interception, and Augmentation
 Philipp A. Hartmann, Malher A. Fakhri, Kim Grütner

A poster session will be organized at FDL to present COMPLEX objectives and current results.

The FDL public that was addressed by the COMPLEX presentation is composed of industry and academic representatives involved in various aspects of system specification and design: high-level graphical specifications with UML, C-based, SystemC modelling, assertion-based dynamic and formal verification, analog and mixed signal modelling.

Industry sectors represented at FDL are: system companies, SoC integrators, IP providers, EDA partners.

ESCUG (European SystemC Users' Group) at FDL 2011

ECSI supported the organization of the ESCUG meeting organized in conjunction with the conference. COMPLEX-related presentations have been given at this meeting by the project partners.

2.3 FDL 2012 – Forum on specification & Design Languages

FDL 2012 will be held September 18-20 in Vienna, Austria. COMPLEX related papers will be presented. In addition, COMPLEX will be featured in the conference program and a Poster Session will be organized at FDL to facilitate the exchange with conference participants.

2.4 ESLsyn 2011 – Electronic System Level Synthesis Conference

Web site: <http://www.ecsi.org/eslsyn2011>

Date & Place: June 5-6, 2011, San Diego, California, USA

Organization: ECSI

Technically co-sponsored by CEDA and IEEE.



Conference Description

The ever increasing need for enhanced productivity in designing highly complex electronic systems drives the evolution of design methods beyond the traditional approaches. Virtual prototyping, design space exploration and system synthesis with the goal of optimized and functionally correct product implementation are needed for designing both HW and SW parts.

The system design teams expect newer and more efficient methods and tools supporting better management of the design complexity and reduction of the design cycle time all together, breaking the trend to compromise on the evaluation of various design implementation options. Designing at higher levels of abstraction is a viable way to better cope with the system design complexity, to verify earlier in the design process and to increase code reuse.

The **Electronic System Level Synthesis Conference ESLsyn** focuses on automated system design methods that enable efficient modelling of systems to provide the

capability to synthesize HW platforms and embedded software with particular aspects related to synthesis.

Target Audience

This conference provides an overview of existing and emerging solutions provided by both industrial partners (EDA companies) and research institutions in the domain of ESL synthesis. It gives an outline of synthesis methods and tools available currently in the market and discusses their applicability, performance, strengths and user experiences. Finally, the event creates a discussion platform for experience exchange between providers of synthesis technology and industry users, but also will be a forum to discuss scientific concepts and paradigms for the future evolution of synthesis methods.

Topics

Cyber-Physical System/System/Platform: model-driven synthesis, models of computation, virtual prototyping, design space exploration, design methodologies, architectures, co-design, interface synthesis, partitioning, performance analysis, optimization, modeling refinement, transformation, generation, languages, formal specification and verification methods, virtualization, target platforms: ASIC, FPGA, GPU, many- & multi-core, SOC platforms, HW accelerators, ...

High-Level Synthesis, Behavioral Synthesis, Architectural Synthesis for HW Design: hierarchical synthesis, algorithmic transformations, loop transformations, scheduling & binding techniques, correctness, formal verification, reliability, incremental synthesis, control-oriented synthesis, low-power synthesis, performance-driven synthesis, target-specific synthesis, multiple clock design, input languages & subsets, internal representation, interaction with low-level synthesis, certification, trade-off analysis, ...

Embedded Software Synthesis: programming models (including multi-core, GPU programming models), correct-by-construction software synthesis, intermediate representations, scheduling techniques, binding, communication and synchronization protocols, middleware/hardware-dependent software, performance analysis and optimization, domain-specific languages and methods (AADL etc.), concurrent program synthesis, compilers for multi-/many- cores, time triggered vs. event triggered models, synchronous programming models, formal methods for embedded software design and verification, ...

Conference Summary

ESLSyn 2011: First ECSI International Symposium on Electronic System Level Synthesis in cooperation with the IEEE Council on Electronic Design Automation (IEEE CEDA) was held on June 5 and 6, 2011 at the San Diego Convention center. The symposium was organized by ECSI with Daniel Gajski (UC Irvine, USA), and Adam Moraweic (ECSI, France) as general chairs. The technical program committee was chaired by Phillip Coussy (Univ. of Bretagne-Sud, France), and Sandeep Shukla (Virginia Tech, USA).

13 papers were selected for presentation at the conference. The presentations were divided into topics including co-design, FPGAs and synthesis, modeling, and system design. In addition to the presentation of these regular papers, there were 4 keynote speeches as well as an invited presentation by Prof. Daniel Gajski entitled "Quo Vadis ESL Synthesis?", which led to very interesting debates and discussions.

Dr. Rishiyur S. Nikhil, CTO of Bluespec, Inc. opened the conference with a keynote titled “Rethinking your Assumptions in ESL Design”, making a very strong case for not using C/C++ like imperative languages as ESL language. The second keynote, presented by Michael McNamara of Cadence Design Systems, discussed the co-dependent relationship of high-level synthesis and verification, elaborating on ECO management and incremental synthesis technologies.

The second day of the conference was opened with a keynote by Andres Takach, chief Scientist of Mentor Graphics, who outlined ESL model refinement challenges, with particular emphasis on C/C++ based ESL. The final keynote speech discussed the synthesis of distributed real-time embedded software with specific connection to PTIDES project and was given by Prof. Edward Lee, distinguished professor at the University of California at Berkeley.

A panel discussion led by Prof. Sandeep Shukla of Virginia Tech, entitled "ESL Synthesis? Get Real!!!", concluded that ESL synthesis is very important for the near future, but what we have now is high-level synthesis of individual components and not system synthesis. More research is needed for system synthesis to become a reality. The panelists included Stephen Neuendorffer from Xilinx, Kim Gruettner from OFFIS, Benjamin Carrion Schafer from NEC Corp., and Johannes Stahl from Synopsys.

Xilinx, Cadence, and Mentor Graphics provided tool demonstrations regarding EDA synthesis solutions that gave the participants of the event a good insight into the state-of-the-art solutions available now for the industrial deployment and used for production chips.

Demo posters were also provided by Xilinx, Cadence, Mentor Graphics, as well as the COMPLEX Project, a European project related to system synthesis methods taking into account power and performance characteristics.

ESLsyn will be a yearly event, gathering the whole community related to system, HW and SW synthesis.

General Chair: Dan Gajski, University of California, Irvine

Co-Chair & Organization: Adam Morawiec, ECSI

Program Co-Chairs: Philippe Coussy, Lab-STICC, Université de Bretagne Sud and Sandeep K. Shukla, Virginia Tech University

Keynote Speakers

- Rishiyur S. Nikhil, Bluespec
- Andres Takach, Mentor Graphics
- Edward Lee, University of California, Berkeley
- Michael McNamara, Cadence Design Systems

Invited Speaker

- Dan Gajski, University of California, Irvine

2.5 ESLsyn 2012 – Electronic System Level Synthesis Conference

Web site: <http://www.ecsi.org/eslsyn>

Date & Place: June 2-3, 2012, San Francisco, California, USA (co-located with DAC)

Organization: ECSI

Technically co-sponsored by CEDA and IEEE.

COMPLEX Related Special Session & Demo

A special session will be held on Sunday, June 3 regarding COMPLEX related topics and presented by COMPLEX Consortia members: Achim Rettberg, University of Oldenburg, William Fornaciari, PoliMi, Franco Fummi, University of Verona. Furthermore, a poster session will be held each day of the conference during which COMPLEX will be featured.

Conference Description

The ever-increasing need for enhanced productivity in designing highly complex electronic systems drives the evolution of design methods beyond the traditional approaches. Virtual prototyping, design space exploration and system synthesis with the goal of optimized and functionally correct product implementations are needed for designing both HW and SW parts. ESL design does not only provide system architects with the right tools to make the right decisions about the system architecture, it includes the methodologies and techniques that correlate the ESL model. A well-connected ESL-to-implementation design flow is needed.

The system design teams expect newer and more efficient methods and tools supporting better management of the design complexity and reduction of the design cycle time all together, breaking the trend to compromise on the evaluation of various design implementation options. Designing at higher levels of abstraction is a viable way to better cope with the system design complexity, to verify earlier in the design process and to increase code reuse.

The **Electronic System Level Synthesis Conference ESLsyn** focuses on automated system design methods that enable efficient modelling of systems to provide the capability to synthesize HW platforms and embedded software with particular aspects related to synthesis.

Target Audience

This conference will provide an overview of existing and emerging solutions provided by both industrial partners (EDA companies) and research institutions in the domain of ESL synthesis. It will give an outline of synthesis methods and tools available currently in the market and discuss their applicability, performance, strengths and user experiences. Finally, the event will create a discussion platform for experience exchange between providers of synthesis technology and industry users, but also will be a forum to discuss scientific concepts and paradigms for the future evolution of synthesis methods.

Topics

ESLsyn will focus on the five key tasks related to the design and verification of complex, programmable electronic products:

- The development of product architectures and specifications, including the incorporation and configuration of IP

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- The mapping of applications to a product specification, including hardware/software partitioning and processor optimization
- The creation of pre-silicon, virtual hardware platforms for software development
- The determination/automation of a hardware implementation for that architecture
- The development of reference models for verifying the hardware

Furthermore, ESLsyn addresses:

- Cyber-Physical System/System/Platform related to ESL design flow
- High-Level Synthesis, Behavioral Synthesis, Architectural Synthesis for HW Design in cooperation with the ESL design flow
- Embedded Software Synthesis that is used into the ESL design flow

Co-located with DAC

The Design Automation Conference (DAC) is the premier event for the design of electronic circuits and systems, and for EDA and silicon solutions. Now in its 49th year, DAC features a wide array of technical presentations, as well as more than 200 of the leading electronics design suppliers in a colorful, well-attended trade show that, literally, attracts stakeholders from around the world.

DAC is where the IC Design and EDA ecosystem learns, networks, and does business. DAC is also where the latest technical research is presented. DAC covers all topics related to the design complex systems on chip: Embedded System design and verification down to physical layout verification & test.

General Co-Chairs:

Sandeep Shukla, Virginia Tech
Philippe Coussy, Lab-STICC

Program Co-Chairs:

Jens Brandt, TU Kaiserslautern
Achim Rettberg, University of Oldenburg

Organization: Adam Morawiec, ECSI

3 Workshops

3.1 2nd Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures

Website: <http://conferences.microlab.ntua.gr/parma2011/>

Date & Place: Lake Como, Italy, February 23, 2011

(Co-located with ARCS 2011 - Architecture of Computing Systems)

Organization: POLIMI

Description:

The current trend towards many-core architecture requires a global rethinking of software and hardware design approaches. The PARMA workshop focuses on parallel programming models, design space exploration and run-time resource management techniques to exploit the features of many-core processor architectures. The PARMA workshop is composed of three main sessions:

- S1: Programming models and languages, compilers and virtualization techniques
- S2: Runtime management, power management and memory management
- S3: Design space exploration and many-core architecture customization

COMPLEX activities:

This workshop organized by POLIMI has the objective to create networking around some of the project activities and to spread-out the knowledge especially focused on design space exploration, programmability, software optimization and estimation and run-time management issues for embedded systems. In this workshop POLIMI will present research and development activities related to COMPLEX.

Organizing Committee

Workshop General Co-Chairs:

Dimitrios Soudris, National Technical University of Athens, Greece

Giovanni Agosta, Politecnico di Milano, Italy

Session Chairs:

S1: Torsten Kempf, ISS-RWTH Aachen University, Germany

S2: Gianluca Palermo, Politecnico di Milano, Italy

S3: Benno Stabernack, Heinrich Hertz Institute, Fraunhofer Institute, Germany

Publicity Chair :

Arindam Mallik, IMEC

Publication Chair:

Carlo Galuzzi, Delft University of Technology

3.2 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications (DEPCP'2011)

Website: <http://conferenze.dei.polimi.it/depcp/2011/index.html>

Date & Place:

March 18, 2011, Grenoble, France (co-located with DATE'11, Friday Workshop W3)

Organization: POLIMI

Description:

The future of embedded computing is shifting to multi/many-core designs to boost performance due to the unacceptable power consumption and operating temperature increase of fast single-core CPU's. Hence embedded system designers are increasingly faced with the following new big challenges: the support for a variety of concurrent applications, and the platform heterogeneity. These challenges lead to the following significant issues:

- How can we write applications that exploit the underlying (parallel) architecture, without burdening the application designer?
- What does the application designer really need to know of the underlying architecture?
- What tools are needed to efficiently map applications and what part of the process should be automated?
- How should we design the underlying architectures?

This workshop brings together researchers actively working on architectures, design tools, and applications for embedded parallel computing platforms to address these questions and related issues.

Topic Areas:

The workshop focused on three main sessions:

- Architectures: on the most relevant problems arising during the design exploration and optimization of many/multi core architectures.
- Design tools: on the state-of-the-art of tool development, showing where we are now and the directions we need to move in.
- Applications: on the analysis, development, modification and integration of applications with respect to parallel computing platforms.

This workshop organized by POLIMI with the support also of IMEC has the objective to create networking around some of the project activities and to spread-out the knowledge especially focused on design space exploration, programmability, software optimization and estimation and run-time management issues for embedded systems. In this workshop POLIMI will present research and development activities related to COMPLEX.

COMPLEX related posters:

- *Audio Driven Video Surveillance System using COMPLEX design flow.*
Fabien Colas-Bigey (Thales), Sara Boccio (ST-I), Chantal Ykman-Couvreur (IMEC), Gianluca Palermo (PoliMi), Philipp A. Hartmann (OFFIS)

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- *Using the COMPLEX Design Flow for Space Domain Applications*
Francisco Ferrero (GMV), Kim Grüttner (OFFIS), Fernando Herrera (UC),
Gianluca Palermo (PoliMi), Bart Vanthournout (SNPS), Emmanuel Vaumorin
(MDS)
- *A Framework for Generic HW/SW Communication using Remote Method
Invocation.*
Philipp A. Hartmann, Philipp Ittershagen, Kim Grüttner, Frank Oppenheimer
(OFFIS), Achim Rettberg, (University of Oldenburg)

Organization:

General Co-Chairs: Cristina Silvano and Giovanni Agosta, Politecnico di Milano, Italy
Architectures Session Chair: Maurizio Palesi, KORE University, Italy
Design Tools Session Chair: Chantal Ykman-Couvreur, IMEC, Belgium
Applications Session Chair: Diana Göhringer, Fraunhofer IOSB, Germany
Poster Session Chair: Michael Hübner, Karlsruhe Institute of Technology, Germany
Panel Session Co-Chairs: Jürgen Becker and Michael Hübner, Karlsruhe
Inst. of Technology, Germany
Web and Posters Submission Chair: Fabrizio Castro, Politecnico di Milano, Italy
Publicity Chair: Maurizio Palesi, KORE University, Italy

3.3 Early Timing and Power Information of Complex SoC Designs using Augmented Virtual Platforms

Web site: <http://complex.offis.de/news/82-date2011#exhibition-theatre-session>

Date & Place: March 17, 2011, Exhibition Theatre at DATE

Rationale and Abstract:

Consideration of an embedded system's timing behaviour and power consumption at system-level is an ambitious task. Sophisticated tools and techniques exist for power and timing estimations of individual components such as custom hard and software as well as IP components. But prediction of the composed system behaviour can hardly be made.

In this session we present the concept of an ESL framework for timing and power aware rapid virtual system prototyping of embedded HW/SW systems. Our proposed flow combines system-level timing and power estimation techniques available in commercial tools with platform-based rapid prototyping. Our proposal aims at the generation of executable virtual prototypes from a functional C/C++ specification. These prototypes are enriched by static and dynamic power values as well as execution times. They allow a trade-off between different platforms, mapping alternatives, and optimization techniques, based on domain-specific workload scenarios.

Presentations:

- *The COMPLEX ESL Framework for Timing and Power Aware Rapid Prototyping of HW/SW Systems*
Kim Grüttner – OFFIS
- *Using Virtual Platforms for Energy Efficient SW-Design*
Bart Vanthournout - Synopsys
- *Automatic Abstraction of RTL IPs into Equivalent TLM Descriptions for Platform Simulation*
Franco Fummi – EDALab
- *Choosing IP-XACT IEEE 1685 standard as a unified description for timing and power performance estimations in virtual platforms*
Emmanuel Vaumoris – Magillem Design Services

3.4 M-BED'2011, the 2nd Workshop on Model Based Engineering for Embedded Systems Design

Web page: <http://www.ecsi.org/m-bed>

Date & Place: March 18, 2011, Grenoble, France (co-located with DATE)

Organization: ECSI



Description:

The application of model-based engineering (MBE) methods for software and systems development in industry is increasing. Moreover, the integration of component-based approaches with MBE has further accelerated its adoption along is also providing a basis for a sounder theoretical underpinning.

The focus of this workshop is on the use of MBE for embedded systems development (e.g. in the industrial transport sector for applications such as railway systems, automotive, aerospace, and related domains). In this context, special focus is given to MARTE, the UML profile for Modelling and Analysis of Real-Time and Embedded systems, which has proven successful in a number of projects. In particular, the program concentrates on the following topics:

- The infrastructure that supports MBE, that is, the requisite languages, tools, and standards, as well as the combination of design and V&V activities, and the diverse engineering disciplines involved in embedded system design.
- Process and methodology related issues, such as guidelines for deciding when and how to use domain-specific languages, appropriate integration of tools, and advanced methods to assist on architecture exploration subjected to multiple non functional constraints.
- Experience with applying MARTE and suggestions of improvements to this standard.

The aim of the workshop is to bring together researchers as well as system designers and tool developers from both industry and academia to discuss applications of model-based engineering in general and MARTE usage in particular. A significant portion of time will be reserved for discussion.

Complementing the accepted paper presentations will be several invited presentations by members of the MARTE standardization task force, specialists participating in relevant European projects, and representatives of MBE tool vendors. The one-day workshop is organized in multiple sessions, each focusing on a particular topic. Rather than have questions at the end of each presentation, all discussion will be conducted at the end of the session, with all presenters in the session responding as a group to questions of the session moderator as well as other attendees.

Organizers:

Pierre Boulet, Univ. Lille, FR
Daniela Cancila, Sherpa Engineering, FR
Sébastien Gérard, CEA-LIST, FR
Adam Morawiec, ECSI, FR
Chokri Mraihda, CEA-LIST, FR
Laurent Rioux, Thales RT, FR
Bran Selic, Malina Software Corp., CA

In this workshop some preliminary results from UC side will be presented regarding the IP-XACT generation from UML/MARTE. Specifically, the following paper will be presented:

Generation of Abstract IP-XACT Platform Descriptions from UML/MARTE for System-Level Performance Estimation.

F.Herrera, E. Villar.

3.5 Workshop on Micro Power Management for Macro Systems on Chip (uPM2SoC)

March 18, 2011, Grenoble, France

Web site: <http://www.ece.cmu.edu/~dianam/uPM2SoC10/>

Date & Place: March 18, 2011, Grenoble, France (co-located with DATE)

Organizers:

Technical program:

Diana Marculescu, Carnegie Mellon University

Suzanne Lesecq, CEA-LETI Minatec

Invited talks:

Diego Puschini, CEA-LETI Minatec

Panel session:

Radu Marculescu, Carnegie Mellon University

Description:

Increased integration of hundreds of processing cores on the same silicon substrate has allowed the concurrent execution of multiple applications on a chip, but at the cost of significant increase in on-chip power consumption. On-chip power management has therefore become a critical component of every step in the many-core design flow, from physical design all the way up to micro-architecture and system-level design. While dynamic power management has been extensively studied for the case of single-core systems, many-core systems present additional challenges that require maintaining appropriate performance levels for applications running on the system both in the context of turning on/off cores and using selectively power states, or in the context of using Dynamic Voltage Frequency Scaling (DVFS) for enabling a certain performance level at a minimum power. Furthermore, enabling power management at macroscale – for hundreds or thousands of on-chip resources – while relying on capabilities developed at microscale – specifically, technology and device-level knobs – becomes an essential for effective power control.

This workshop addresses this need by targeting emerging topics in power management and control of large scale many-core systems, such as scalability, distributed vs. centralized vs. hybrid approaches, as well as technology-driven challenges that need to be considered for providing a truly power-aware solution, such as static and dynamic variations and reliability, as well as limits for control strategies for technologies 22nm and beyond.

COMPLEX related poster:

- *Enabling Timing and Power Aware Virtual Prototyping of HW/SW Systems.*
Kim Grüttner, Kai Hylla, Sven Rosinger, Philipp A. Hartmann, Wolfgang Nebel, OFFIS.

3.6 Embedded Software Development on Virtual Platforms – Ready for Prime Time?

Web site:

<http://www.ecsi.org/workshop2012/embedded-sw-development-virtual-platforms>

Date & Place: February 28, 2012, Nuremburg, Germany (at Embedded World)

Organization: ECSI



Organizers:

Adam Morawiec, ECSI, France

Frank Oppenheimer, OFFIS, Germany

Motivation:

Embedded software development process and methodologies aims today mainly at simple single-core platforms. Due to power constraints today's high performance platforms are dominated by multi-core and heterogeneous architectures. To efficiently exploit these platforms in the software development process we need to carefully consider the platform artefacts, features and strengths.

Current software development process is not efficient anymore because of:

- Long overall development time of software starting late after the underlying hardware platform is available
- Difficult debugging, testing and validation of software on complex hardware platforms
- Optimized usage of available resources (hardware, low-level software, ...)
- Cost of optimization, re-spins, bug fixing in both software and hardware

Virtual Platforms offer a viable and powerful solution to the above weaknesses.

Description:

Development and integration of embedded software executing on a hardware platform is increasingly becoming a key factor in product differentiations well as in its final market success or failure. Not only does the software development process determine the overall product functionality, it also significantly influences its entire development time. If the software is finished too late then the entire product can fail.

In addition software complexity is growing and consumes significant development and verification time. Add to this the trend towards multi-core architectures today, which makes them challenging to analyze and debug, and it should come as no surprise that recent studies show that software development effort already surpasses the effort spent on hardware for a typical 90nm SoC design. Furthermore, software becomes an integral part of any system verification concept, as only the combination of hardware and software allows verifying system functionality.

With an ever growing system complexity the industry needs to apply new concepts, paradigms and methods for embedded software development and hardware/software system validation that will be able to tackle with the problems of quality and correctness, providing significant gain in the design productivity and shorten time to market.

It is the belief that such a new way of development will be based on **embedded software development on virtual platforms**. The concept of system virtualization has been around for almost a decade, during which time the industry started to learn how to build and apply these technologies. Topics of controversy have been the necessary accuracy vs. possible simulation performance, the need for a system-level IP eco system, and the move from tool-specific simulation paradigms towards public standards.

This workshop will cover the state-of-the-art of embedded software development on virtual platforms. This includes technologies and tool environments for building, executing and distributing virtual platforms. It will address existing and upcoming industry standards. Significant room will be given to cover user experience, both from those building virtual platforms, as well as from those deploying virtual platforms for embedded software development, or software-driven system validation.

Lessons learned, problems solved, remaining issues will be shared with the participants.

Target Audience:

- Embedded software developers: application, hardware dependent software, and driver developers
- Embedded system developers
- Software verification engineers
- Virtual platform developers

COMPLEX related presentations:

Software Simulation Technologies in Virtual Platforms

Eugenio Villar, University of Cantabria, Spain

The COMPLEX Virtual Platform Design Approach for Performance and Energy Efficient Embedded Systems: A European Research Perspective

Frank Oppenheimer, OFFIS, Germany

COBRA, Using a Virtual Platform for the Design of a Programmable Wireless Baseband System

Jeroen Declerck, IMEC, Belgium

Virtual Platform Eco-System: Tools, IPs and Services Demonstrations:

- Cadence
- Carbon Design Systems
- CoSynth
- EDALab (COMPLEX partner)
- Lauterbach
- Magillem (COMPLEX partner)

3.7 Quo Vadis, Virtual Platforms? Challenges and Solutions for Today and Tomorrow (QVVP12)

Website: <http://qvvp12.offis.de>

Date & Place: March 16, 2012, Dresden, Germany (co-located with DATE)

Organizers:

Rainer Leupers, RWTH Aachen University, DE

Christian Haubelt, University of Rostock, DE

Achim Rettberg, Carl von Ossietzky University Oldenburg, DE

Kim Grüttner, OFFIS – Institute for Information Technology, DE

Rationale and Abstract

Nowadays, the deployment of Virtual Platform models is an industry-proven technique in a wide variety of design tasks from pre-silicon software development to performance analysis and exploration. With the increasing complexity, both in terms of the applications and the target platforms (e.g. increasing number of cores, more complex memory hierarchies), the Virtual Platform per se is not an answer to all of today's design challenges. But by adding further abstraction to the models, an increasing need for automated mapping, refinement, and model transformations is needed. Formal, static, and dynamic analysis methods are increasingly dependent on platform details, requiring traceability during all design phases.

This workshop aims to bring together developers, researchers, and managers from industry and academia to develop a perspective for the future use of Virtual Platforms by exchanging knowledge about current and future requirements and their possible solutions. The workshop will also provide some space for the provision of state of the art and tangible results and session on tool demos.

Questions addressed during the workshop are:

- How to efficiently generate a Virtual Platform for new applications and HW platforms?
- How to close the implementation/refinement gap?
- Which properties of a real system can be captured?
- What are the requirements for future Virtual Platforms?
- How can Virtual Platforms support the development of future real-time applications for MPSoCs?

In this workshop, different points of view have been discussed by

- potential users of Virtual Platforms from different domains
- tool vendors already offering Virtual Platform tools and modeling techniques, and
- academic research institutes from around the world showing recent progress in Virtual Platform synthesis and core technologies.

Who attended?

This Friday Workshop gave an extensive overview on research directions around Virtual Platforms, covering system and Virtual Platform synthesis, Timing and Power modeling using Virtual Platforms, and support for the development of hard real-time applications on multi-core Platforms. The workshop has been visited by researchers and professionals who wanted to get an insight in future design methodologies as well as managers who wanted to acquire a basic knowledge on the usage of Virtual Platforms.

Number of participants: ~50

Workshop Format and Structure

The workshop presentations have been by invitation, an open call has been issued for poster session presentations. Poster submissions for each topic area have been reviewed by the workshop organizers and the invited speakers respectively.

COMPLEX related presentations:

Task Modeling and HW/SW partitioning for System Performance Optimization

Tim Kogel – Synopsys, DE

High-Level Synthesis, TLM Power State Machines, and advanced tracing for Virtual Platforms

Philipp A. Hartmann – OFFIS – Institute for Information Technology, DE

3.8 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications (DEPCP'2012)

Website: <http://conferenze.dei.polimi.it/depcp/>

Date & Place:

March 16, 2012, Dresden, Germany (co-located with DATE'12)

Organization: POLIMI

Description:

Embedded computing is shifting to multi/many-core designs to boost performance due to unacceptable power consumption and operating temperature increase of fast single-core CPU's. Hence, embedded system designers are increasingly faced with several big challenges, namely: the support for a variety of concurrent applications, and the platform heterogeneity. These challenges lead to the following significant design issues:

- How can applications that exploit the underlying (parallel) architecture be written without burdening the application designer?
- What does the application designer really need to know of the underlying architecture?
- What tools are needed to efficiently map applications and what part of the mapping process should/could be automated?
- How should we design and optimize the underlying architectures?

This workshop brings together researchers and practitioners actively working on architectures, design tools, and applications for embedded parallel computing platforms to address these questions and related issues.

Topic Areas:

The workshop will have three main **topic areas**:

- **Architectures:** on the most relevant problems arising during the design exploration and optimization of many/multi core architectures.
- **Design tools:** on the state-of-the-art of tool development, showing where we are now and the directions we need to move in.
- **Applications:** on the analysis, development, modification and integration of applications with respect to parallel computing platforms.

COMPLEX related posters:

- *Energy-aware run-time management in video surveillance systems*
Laurent San ([Thales](#)), Sara Bocchio ([ST-I](#)), Chantal Ykman-Couvreur ([IMEC](#)),
Gianluca Palermo ([PoliMi](#)), Philipp A. Hartmann ([OFFIS](#))

Organization:

General Co-Chairs: Cristina Silvano and Giovanni Agosta, Politecnico di Milano, Italy,
and Joao Cardoso, Universidade do Porto, Portugal

Architectures Poster Session Chair: Maurizio Palesi, KORE University, Italy

Design Tools Session Chair: Chantal Ykman-Couvreur, IMEC, Belgium

Applications Session Chair: Diana Göhringer, Fraunhofer IOSB, Germany

Posters Submission Chair: Dimitris Mpekiaris, National Technical University of
Athens, Greece

Publicity Chair: Maurizio Palesi, KORE University, Italy

4 Web Educational Material

EDALab created a web site for the HIFSuite tool developed in the COMPLEX project (<http://www.hifsuite.com>) and from this web site interested people can download a demo version with a presentation, a tutorial, a some exercises to learn how to use the tool.

EDALab, as a spin-off of the University of Verona, has strict relationships with academic educational activities which are considered a source of scientific inspiration and a way to test the developed tools.

HIFSuite is used inside the laboratory of embedded system design to support both teaching and research activities. Under-graduate students and PhD students learn how to use HIFSuite for their educational activity and its internal architecture to modify it by adding/improving features.

Another tool developed by EDALab in the COMPLEX project is the SystemC Network Simulation Library (SCNSL). SCNSL has been released on SourceForge as open source software to enforce its use and the study of its internal structure. In the last year, a great effort has been devoted to the creation of SCNSL manual which explains how to use and modify the simulation library. SCNSL is used in the under-graduate class of Networked Embedded Systems to learn their design flow. It is also used in a significant number of master and PhD thesis about the design of networked embedded systems such as wireless sensor networks and networked control systems.

In the last year, EDALab spent a non-negligible effort to standardize the generation of documentation for its tools. A standard structure for the manuals has been defined, a wiki and a content management system have been set up to store information for the users.

In the future, EDALab will increase the use of its tools as training support not only inside the University of Verona but also towards companies to create new economical opportunities.

5 Lectures & University Courses

5.1 Low Energy System Design

Course offered at: Carl von Ossietzky University Oldenburg

Course interval: It is offered every winter semester.

Date of 1st pass: October 2010- February 2011

Date of 2nd pass: October 2011- February 2012

Link: <http://ehs.informatik.uni-oldenburg.de/42686.html>

Organization:

Axel Reimer - Carl von Ossietzky University Oldenburg

Domenik Helms – OFFIS

Patrick Knocke – OFFIS

Malte Metzdorf – OFFIS

Sven Rosinger – OFFIS

Kiril Schröder - Carl von Ossietzky University Oldenburg

Description:

This lecture gives an introduction to the topics of power estimation and power optimisation for integrated circuits. During this course students will:

- get insight into the general problem of power dissipation (dynamic and static) and its main sources in today's transistor technology
- acquire a deep knowledge of requirements-driven design of embedded systems
- get knowledge of state-of-the-art power analysis and power optimization techniques
- get practical experience using design and analysis tools for power
- get practical experience with low power design flow

COMPLEX related contents:

Beside a general introduction of power estimation and optimisation, the lecture presents COMPLEX relevant topics. Furthermore, project results are directly integrated into the lecture. In summary, the lecture covers the following project related contents:

- software-power estimation basics
- soft- and hard-macro models for RT-level components
- model generation and data abstraction techniques
- RTL datapath and controller synthesis
- system-level estimation techniques being developed in the COMPLEX project
- presentation of the BAC++ annotation technique for functional- as well as non-functional power and delay estimates

5.2 System-Level Design

Course offered at: Carl von Ossietzky University Oldenburg

Course interval: It is offered every summer semester.

Date of 1st pass: April 2011 – July 2011

Date of 2nd pass: April 2012 – July 2012

Link: <http://ehs.informatik.uni-oldenburg.de/42687.html>

Organization:

Kim Grüttner – OFFIS

Philipp A. Hartmann – OFFIS

Ralph Görden – OFFIS

Description:

This master course extends the basic courses on embedded system that give an overview on the design of hardware/software systems. It covers state-of-the-art methods and tools for the design of today's systems. In a practical part, an introduction to SystemC is given, which is otherwise not covered in depth at the University of Oldenburg. Based on SystemC, the modelling of virtual prototypes at Transaction-Level is given. The course covers the following topics in detail:

- Phases of a System-Level Design Flow
- Refinement and Transformation of an initial specification towards a real implementation
- Current design methods and tools
- (Formal) Models of Computation used for specification and analysis
- Partitioning and parallelisation of applications
- Evaluation and exploration of design decisions
- Modelling of system components and architectures based on system-level design languages (SpecC, SystemC)

COMPLEX related contents:

Besides a general introduction to system-level design in general, the lecture presents COMPLEX relevant topics. Furthermore, project results are directly integrated into the lecture. In summary, the lecture covers the following project related contents:

- Transaction-level modelling of applications and architectures
- Modelling and abstraction of extra-functional properties of a system
- Design-Space Exploration techniques and tools
- Virtual prototyping in SystemC

6 Planned Activities

In addition to the already performed activities, future training activities and workshops are planned in the remaining period of the project. These activities can be categorized in the same categories as seen in earlier sections of the report.

6.1 Conferences

The activities listed in this section are separate from dissemination activities addressed by the deliverables in Task 5.2 and are aimed at providing additional training and education activities mainly for industry audience.

During the **Embedded Systems Week 2012** in Tampere Finland (<http://www.esweek.org>), the COMPLEX project plans to offer a **special session** presenting the main results of the project. The proposed contents are as follows:

System-Level Power Modeling, Analysis and Optimization using Virtual Platforms

- *SW-Centric System Specification and executable Model generation*
(GMV,UC)
- *High-level software energy and timing estimation of embedded applications*
(PoliMi)
- *Custom Hardware Timing and Power Estimation using High-Level Synthesis*
(OFFIS, UC)
- *Non-intrusive IP-Component Executable Timing and Power Representation using Protocol and Power State Machine*
(OFFIS, ST-I)
- *Dynamic Resource Management for Power Management at System-Level*
(IMEC, PoliMi, Thales)
- *Virtual Platform Integration and Extension for Extra-Functional Properties*
(OFFIS, SNPS)

6.2 Workshops

ECSI will continue to organize in a regular way the workshop at Embedded World in Nuernberg, Germany on Virtual Platforms. The main motivation to maintain this event is that EW attracts audience from embedded SW development area (companies and research centers) that are not usually present at the traditionally microelectronics and EDA related events like DAC or DATE.

In addition, there are two aspects that we identified to be addressed:

- Virtual Platform construction – how to build Virtual Platform from models of IPs available from several different sources, how to successfully integrate them and build low-level SW (Hardware-dependent SW) associated with the platform, how to provide configuration and parameterization capabilities, how to model at higher level performance characteristics (directly related to COMPLEX objective)

- The other area concerns the embedded SW developers: once Platform model is available, its HW implementation can start (usually RTL development), but the same model can be used by application SW developers, who may fully execute their SW on Virtual Platform, and by this validate SW functionally and check performance and interaction with lower-level SW (drivers) and HW components

6.3 Lectures & University Courses

OFFIS will continue to incorporate new COMPLEX results and contents to the regular COMPLEX-related courses given at the University of Oldenburg (Low-Energy System Design, System-Level Design). Especially the demonstrations and webinar contents (see Section 6.5) will be added to the curriculum, to give an insight to state-of-the-art research results to the students in the courses.

6.4 Summer Schools

COMPLEX Project plans to participate in the Summer School on European projects results exchange. It is a plan among several European projects to organize a working week to share results between on-going projects. More information will be provided in the next report.

6.5 Training Webinars

In order to further disseminate the COMPLEX results, several online webinars demonstrating the COMPLEX tools and methods are planned. These webinars will be made available to the general public via the COMPLEX project website at <http://complex.offis.de> in terms of pre-recorded video presentations for on-demand download.

Table 1: List of COMPLEX Webinars

COMPLEX Training Webinars	
Partner	Title
OFFIS	Introduction to the COMPLEX Design, Estimation, and Exploration Flow
OFFIS	Modelling extra-functional properties with Power State Machines in SystemC TLM-2.0
OFFIS	Custom Hardware Timing and Power Estimation using High-Level Synthesis
OFFIS	Composable ESL Timing and Power Simulation for Composable SoC Design

Further topics will be made available, e.g. based on talks given at other events like workshops and tutorials. The existing slides can be used as a basis to prepare a recorded talk, available for download on-demand.