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COdesign and power Management in PLatform-based design space EXploration

Project Duration 2009-12-01 – 2013-03-31 Type IP

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<tr>
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<th>Deliverable no.</th>
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Final Report on Standardization and Dissemination Activities

Prepared by Adam Morawiec, Ana Pinzari (ECSI), All
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<td>0.8</td>
<td>2013-02-26</td>
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<td>AP</td>
<td>0.9</td>
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<td>67</td>
<td>Consolidate inputs, complete draft provided for internal review</td>
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1 Introduction

This document summarizes all dissemination and standardization activities that were undertaken by the COMPLEX project consortium as a whole and by each individual partner of the consortium in the whole duration of the project execution. It describes all dissemination activities of the COMPLEX project including activities that were oriented to promote the project, educate on the project achievements and the new scientific and industrial context of the project development.

In the last period of COMPLEX, the consortium intensified efforts to largely present project results to the entire community. Several activities like the tutorial presentation at DATE or the COMPLEX-centric workshop at Embedded World conference were presenting achievements of COMPLEX in a complete and comprehensive way, and their organization was possible only in the final stage of the project, with the effort of the whole consortium.

The deliverable on training activities D5.1.2 presents in detail the educational activities of the project, that are aiming at educating the whole community (understood as industrial and scientific community) on the technical, scientific and practical outcomes of the project and focuses on presentations, tutorials and demonstrations. Certainly, there are several activities like organization of conferences and workshops that can be understood as both education/training activities and larger dissemination activities. Thus, the clear separation of the content of the two deliverables was not always possible. The editors of the deliverables took the position that each of the documents is independent and self-contained and can be read separately from the other. This explains a certain overlap between the two deliverables.
1.1 Scope

This document corresponds to the output deliverable of tasks 5.2 “Standardization” and 5.3 “Dissemination” for the work package 5 within the COMPLEX project (see DoW [1]).

This is a public document that describes the standardization activities and the interface with the appropriate standardization bodies to manage the elaboration and review of standards proposals, and the interaction with the related Working Groups. This document is also devoted to present dissemination activities that were undertaken by the consortium to ensure the visibility and awareness of the project results and to support the adoption of the project results to the maximum extent possible in the industry and research institutions.
1.2 Acronym List

The following table lists all the acronyms used along this document:

Table 1-1: Acronym list

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>DoW</td>
<td>Description of Work</td>
</tr>
<tr>
<td>ECSI</td>
<td>Electronic Chips and System design Iniciative</td>
</tr>
<tr>
<td>MDA</td>
<td>Model Driven Architecture</td>
</tr>
<tr>
<td>OSCI</td>
<td>Open SystemC Initiative</td>
</tr>
<tr>
<td>PDM</td>
<td>Platform Dependent Model</td>
</tr>
<tr>
<td>PIM</td>
<td>Platform Independent Model</td>
</tr>
<tr>
<td>PSM</td>
<td>Platform Specific Model</td>
</tr>
<tr>
<td>RTES</td>
<td>Real-Time Embedded System</td>
</tr>
<tr>
<td>TBC</td>
<td>To Be Completed</td>
</tr>
<tr>
<td>TBD</td>
<td>To Be Defined</td>
</tr>
<tr>
<td>UML</td>
<td>Unified Modeling Language</td>
</tr>
</tbody>
</table>
1.3 Glossary

The following table summarizes the most important concepts provided along this document:

<table>
<thead>
<tr>
<th>Definition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDL</td>
<td>Forum on specification and Design Languages, ECSI conference, <a href="http://www.ecsi.org/fdl">www.ecsi.org/fdl</a></td>
</tr>
<tr>
<td>IP-XACT</td>
<td>Design data representation standard, maintained by Accellera organisation, previously within the SPIRIT Consortium</td>
</tr>
<tr>
<td>M-BED</td>
<td>Model Based Engineering for Embedded Systems Design, workshop organised by ECSI within ECSI MARTE Users’ Group</td>
</tr>
<tr>
<td>MARTE</td>
<td>Modeling and Analysis of Real-Time and Embedded Systems</td>
</tr>
<tr>
<td>OCP-IP</td>
<td>Open Core Protocol International Partnership</td>
</tr>
</tbody>
</table>
2 Dissemination Activities

This section describes the dissemination paths of the exploitable results included in document [2] for the COMPLEX project. The groupings are as follows:

- Submission to standardization bodies (see Section 3 for a detailed description).
- Publication of project results and attendance to conferences.
- Organisation of open workshops and attendance to external workshops.
- Generation of electronic material and deployment of a web-based e-platform.
- Promotion and e-mailing of open results through the ECSI contact lists.

A summary table is provided at the end of this section. For completeness, project results that will utilize multiple dissemination paths appear under multiple dissemination path categories.

2.1 Conferences

The following COMPLEX project results disseminated as published specifications in order that other technology vendors and industrial embedded systems development organisations are able to create tools and platforms that exploit COMPLEX technologies.

2.1.1 FDL 2010 – Forum on specification & Design Languages

Web site:  http://www.ecsi.org/fdl2010
Date & Place: September 14-16, 2010 – Southampton, UK.
Organization: ECSI
Description:
Forum for Design Languages (FDL) is a well-established international forum devoted to dissemination of research results, practical experiences and new ideas in the application of specification, design and verification languages to the design, modeling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems. Several technical areas have been addressed:


**Language Based System Design (LBSD)** – addresses language-based modeling and design techniques for simulation, debugging, transformation, and analysis of hardware/software embedded systems.

**Assertion Based Design, Verification & Debug (ABD)** – welcomes research contributions, tool demonstrations, reports on standardization activities and effective applications in all aspects of innovative property expression and processing, with an emphasis on frontier design levels, verification, automatic synthesis and mechanized design aids.

**Embedded Analog and Mixed-Signal System Design (EAMS)** – addresses design, modeling and verification of analog/mixed-signals systems.

COMPLEX project presented several related papers:

**Session ABD, Tuesday, September 14**
*Mapping of Concurrent Object-Oriented Models to Extended Real-Time Task Networks*,
Matthias Büker, Kim Grüttner, Philipp A Hartmann and Ingo Stierand

**Session LBSD, Tuesday, September 14**
*Towards an ESL Framework for Timing and Power Aware Rapid Prototyping of HW/SW Systems*,
Kim Grüttner, Kai Hylla, Sven Rosinger and Nebel Wolfgang.

**Session ABD+LBSD, Wednesday, September 15**
*Formal Support for Untimed SystemC Specifications: Application to High-level Synthesis*,
Eugenio Villar, Fernando Herrera and Victor Fernandez.

*Modeling of Communication Infrastructure for Design-Space Exploration*,
Franco Fummi, Davide Quaglia, Francesco Stefanni and Giovanni Lovato.

**Session UMES, Thursday, September 16**
*Formal Foundations for MARTE-SystemC Interoperability*,
Pablo Peñil, Fernando Herrera and Eugenio Villar.

A **poster session** was organized in order to present COMPLEX objectives and current results.
2.1.2 FDL 2011 – Forum on specification & Design Languages

Date & Location:  September 13-15, 2011 – Oldenburg, Germany.
Organization:  ECSI

COMPLEX Project presented several related papers at the conference:

**Session UMES, Wednesday, September 14**
*A Framework for the Generation from UML/MARTE Models of IP-XACT HW Platform Descriptions for Multi-Level Performance*
Fernando Herrera and Eugenio Villar.

**Session LBSD, Wednesday, September 14**
*Impact Simulation of Changes to Development Processes: An ESL Case Study*
Frank Poppen, Roland Koppe, Axel Hahn and Kim Grütter.

**Session LBSD, Thursday, September 15**
*SystemC Refinement of Abstract Adaptive Processes for Implementation into Dynamically Reconfigurable Hardware*
Fernando Herrera, Eugenio Villar and Philipp A. Hartmann

**ESCUG Meeting, Tuesday, September 13**
*Non-intrusive TLM-2.0 Transaction Observation, Interception, and Augmentation*
Philipp A. Hartmann

The FDL public that was addressed by the COMPLEX presentation is composed of industry and academic representatives involved in various aspects of system specification and design:
high-level graphical specifications with UML, C-based, SystemC modelling, assertion-based
dynamic and formal verification, analog and mixed signal modelling.

Industry sectors represented at FDL are: system companies, SoC integrators, IP providers,
EDA partners.

**ESCUG (European SystemC Users’ Group) at FDL2011**

ECSI supported the organization of the ESCUG meeting organized in conjunction with the
conference. COMPLEX-related presentations have been given at this meeting by the project partners.
2.1.3 FDL 2012 – Forum on specification & Design Languages

Date & Location: September 18-20, 2012 - Vienna, Austria
Organization:  ECSI

COMPLEX related paper was presented:

Session UMES, Wednesday, September 19
A model-driven methodology for the development of SystemC executable environments,
F Herrera, P Peñil, H Posadas and E Villar.

In addition, COMPLEX featured in the conference program and a Poster Session was organized in order to facilitate the exchange with conference participants.
2.1.4 DATE 2011 – Design, Automation & Test in Europe

**Web site:**  
[https://complex.offis.de/news/82-date2011](https://complex.offis.de/news/82-date2011)

**Date & Location:** March 14-18, 2011 – Grenoble, France

The COMPLEX project initiated the organisation of the presence at the DATE Conference 2011. There will be several ways in which COMPLEX has presented its approach and early results achieved until then:

- Booth in the European Projects exhibition area
- Presentation at the Proposal for DATE 2011 Exhibition Theatre Session (see Section 2.3.3):
  
  *Early Timing and Power Information of Complex SoC Designs using Augmented Virtual Platforms*
- M-BED 2011 Workshop (see Section 2.3.4)
- Magillem company booth

2.1.5 DATE 2012 – Design, Automation & Test in Europe

**Web site:**  

**Date & Location:** March 12-16, 2012 – Dresden, Germany.

The COMPLEX project was present at DATE for the second year with a booth in the European Projects exhibition area. The main COMPLEX objectives were presented:

- Highly efficient and productive design methodology and holistic framework for design space exploration of embedded HW/SW systems.
- Combination and augmentation of well-established ESL synthesis & analysis tools into a seamless design flow enabling performance & power aware virtual prototyping of the HW/SW system.
- Interfacing next-generation model-driven SW design approach and industry standard model-based design environments.
- Multi-objective co-exploration for assessing design quality and optimizing the system platform with respect to performance, power, and reliability metrics.
- Fast simulation and assessment of the platform at ESL with up to bus-cycle accuracy at the earliest instant in the design cycle.
- Optimization benefits from run-time mode adaptation techniques, such as dynamic power management or application adaptation to varying workloads.

**COMPLEX related papers:**

*Application-Specific Memory Partitioning for Joint Energy and Lifetime Optimization*, Haroon Mahmood, Massimo Poncino, Mirko Loghi and Enrico Macii

COMPLEX related workshops at DATE include:

W2 Quo Vadis, Virtual Platforms? Challenges and Solutions for Today and Tomorrow (QVVP'2012)  
http://qvvp12.offis.de

W3 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools and Applications (DEPCP'2012)  
http://conferenze.dei.polimi.it/depcp/

As a DATE sponsor, ECSI printed and distributed a 2-page COMPLEX flyer in 1,200 delegate bags at DATE along with additional flyers distributed at the project booth.
2.1.6 DATE 2013 – Design, Automation & Test in Europe

**Web site:** [https://complex.offis.de/news/94-date2013/#tutorial](https://complex.offis.de/news/94-date2013/#tutorial)

**Date & Location:** March 18-22, 2013 – Grenoble, France

**Tutorial presentation: Advanced Techniques for Power-Aware System-Level Prototyping**

In the design of embedded systems extra-functional properties like timing and power need to be considered during the entire design process. Often these properties can only be estimated after manually implementing a design for a certain target platform and using component-level timing and power analysis tools. At the same time, exploration, analysis, and optimization of embedded applications running on today’s platforms require fast and early virtual system models enabling the consideration of extra-functional properties under real-world application scenarios.

With a group of experts from industry and academia, the tutorial discussed the major challenges and presented novel and innovative research results including tool support to create timing and power-aware Virtual Platforms.

In this context, the following key aspects were covered:

- Model-driven design and automatic platform performance and power model synthesis, enabling early design space exploration
- Efficient application mapping onto resource-constrained platform models
- Early and automatic timing and power estimation for embedded software and custom hardware components, suitable for integration into Virtual Platform models
- RTL-to-TLM re-synthesis and abstraction of timing and power properties, suitable for integration into Virtual Platform models

**COMPLEX Tutorial Programme:**

- *Introduction and tutorial overview* (Frank Oppenheimer, OFFIS)
- *Virtual Platform Generation, Integration and Extension of Extra-Functional Properties* (Tesnim Abdellatif, Emmanuel Vaumorin, MDS)
- *Industrial experience report for model-based design in space/aerospace applications (demo)* (Raúl Valencia, Francisco Ferrero, GMV)
- *From RTL IP to Functional System-Level Models with Extra-Functional Properties* (Davide Quaglia, EDAlab)
- *High-Level Synthesis-based Hardware Power and Timing Estimation* (Philipp A. Hartmann, OFFIS)
- *Software Power and Timing Estimation* (Carlo Brandolese, PoliMi)
- *Network-aware Design-Space Exploration of a Power-Efficient Embedded Application (demo)* (Sara Bocchio, STI)
- *Summary and Closing remarks* (Frank Oppenheimer, OFFIS)

The presentations were accompanied by concrete tool introductions and demonstrations, showing how the presented concepts support improvement of today’s state-of-the-art system-level design flows.
Organizers:
- Frank Oppenheimer (OFFIS)
- Eugenio Villar (UC)
- Philipp A. Hartmann (OFFIS)
- Adam Morawiec (ECSI)

Speakers:
- Eugenio Villar, Universidad de Cantabria, ES
- Davide Quaglia, EDALab, IT
- Emmanuel Vaumorin, Magillem, FR
- Francisco Ferrero, GMV AD, ES
- Carlo Brandolese, Politecnico di Milano, IT
- Philipp A. Hartmann, OFFIS, DE
- Sara Bocchio, STMicroelectronics, IT

Motivation
Power consumption is the limiting physical factor of many current and future systems, especially in the growing mobile computing market. Consequently, successfully mastering the trade-offs between performance and power efficiency is required for future innovative and competitive products. The presented results have been developed in a series of collaborative European research projects and have been integrated into a holistic reference design flow during the COMPLEX project, to be completed in March 2013. During the last phase of this project a wide set of methods and tools have been applied successfully in different domains in mobile computing: Healthcare, Space, Security, and mobile communication. In a full-day tutorial, the COMPLEX reference framework, including industrial experience reports and the integration of latest findings into commercial tools, will be presented in a consistent way.

Objectives
Participants will take a broad knowledge of today’s state-of-the-art concepts, key technologies, and tools for efficient application mapping; platform exploration, selection and configuration based on Virtual Platforms; as well as static and dynamic abstraction, estimation and analysis methods for system-level models including extra-functional properties like power consumption. This enables the attendees to adopt new concepts in competitive industrial R&D or to explore future directions of academic research.

Audience
The tutorial is targeted towards academic researchers and industrial practitioners concerned with system-level design and exploration of embedded applications efficiently running on heterogeneous, power-constrained multicore architectures. At a broader scale, it will be of interest to the majority of DATE attendees working on Embedded System Design in general.

COMPLEX related publications:
A Meta-Model Assisted Coprocessor Synthesis Framework for Compiler/Architecture Parameters Customization,
Sotirios Xydis, Gianluca Palermo, Vittorio Zaccaria and Cristina Silvano.
COMPLEX Project Booth at DATE Exhibition

The COMPLEX project was presented at the exhibition with a dedicated booth to give an overview of the achievements of the project close to its completion.

The main COMPLEX objectives have been:

- Highly efficient and productive design methodology and holistic framework for design space exploration of embedded HW/SW systems.
- Combination and augmentation of well established ESL synthesis & analysis tools into a seamless design flow enabling performance & power aware virtual prototyping of the HW/SW system.
- Interfacing next-generation model-driven SW design approach and industry standard model-based design environments.
- Multi-objective co-exploration for assessing design quality and optimizing the system platform with respect to performance, power, and reliability metrics.
- Fast simulation and assessment of the platform at ESL with up to bus-cycle accuracy at the earliest instant in the design cycle.
- Optimization benefits from run-time mode adaptation techniques, such as dynamic power management or application adaptation to varying workloads.

Magillem Design Services had provided demos on the IP-XACT tool suite dedicated to virtual platform management. It was also presented how high level descriptions in MARTE (or other UML profiles dedicated to systems like SYSML, AUTOSAR, etc.) are managed and assembled using IP-XACT (IEEE 1685 standard), which serves for SystemC netlist generation.

Figure 1 DATE’2013 COMPLEX booth at the exhibition.
2.1.7 ESLsyn 2011 – Electronic System Level Synthesis Conference

Web site:  http://www.ecsi.org/eslsyn2011
Date & Place: June 5-6, 2011, San Diego, California, USA (co-located with DAC)
Organization: ECSI

Description
The system design teams expect newer and more efficient methods and tools supporting better management of the design complexity and reduction of the design cycle time all together, breaking the trend to compromise on the evaluation of various design implementation options. Designing at higher levels of abstraction is a viable way to better cope with the system design complexity, to verify earlier in the design process and to increase code reuse.

The Electronic System Level Synthesis Conference ESLsyn focuses on automated system design methods that enable efficient modelling of systems to provide the capability to synthesize HW platforms and embedded software with particular aspects related to synthesis.

Target Audience
This conference provides an overview of existing and emerging solutions provided by both industrial partners (EDA companies) and research institutions in the domain of ESL synthesis. It gives an outline of synthesis methods and tools available currently in the market and discusses their applicability, performance, strengths and user experiences. Finally, the event creates a discussion platform for experience exchange between providers of synthesis technology and industry users, but also will be a forum to discuss scientific concepts and paradigms for the future evolution of synthesis methods.
Topics

Cyber-Physical System/System/Platform: model-driven synthesis, models of computation, virtual prototyping, design space exploration, design methodologies, architectures, co-design, interface synthesis, partitioning, performance analysis, optimization, modeling refinement, transformation, generation, languages, formal specification and verification methods, virtualization, target platforms: ASIC, FPGA, GPU, many- & multi-core, SOC platforms, HW accelerators.

High-Level Synthesis, Behavioral Synthesis, Architectural Synthesis for HW Design: hierarchical synthesis, algorithmic transformations, loop transformations, scheduling & binding techniques, correctness, formal verification, reliability, incremental synthesis, control-oriented synthesis, low-power synthesis, performance-driven synthesis, target-specific synthesis, multiple clock design, input languages & subsets, internal representation, interaction with low-level synthesis, certification, trade-off analysis.

Embedded Software Synthesis: programming models (including multi-core, GPU programming models), correct-by-construction software synthesis, intermediate representations, scheduling techniques, binding, communication and synchronization protocols, middleware/hardware-dependent software, performance analysis and optimization, domain-specific languages and methods (AADL etc.), concurrent program synthesis, compilers for multi-/many- cores, time triggered vs. event triggered models, synchronous programming models, formal methods for embedded software design and verification.

COMPLEX related publication:


COMPLEX Project provided a demo and a poster related to system synthesis methods taking into account power and performance characteristics.
2.1.8 ESLsyn 2012 – Electronic System Level Synthesis Conference


Date & Place: June 2-3, 2012, San Francisco, California, USA (co-located with DAC)

Organization: ECSI

Description

ESLsyn focused on the five key tasks related to the design and verification of complex, programmable electronic products:

- The development of product architectures and specifications, including the incorporation and configuration of IP
- The mapping of applications to a product specification, including hardware/software partitioning and processor optimization
- The creation of pre-silicon, virtual hardware platforms for software development
- The determination/automation of a hardware implementation for that architecture
- The development of reference models for verifying the hardware

Furthermore, ESLsyn addressed:

- Cyber-Physical System/System/Platform related to ESL design flow
- High-Level Synthesis, Behavioral Synthesis, Architectural Synthesis for HW Design in cooperation with the ESL design flow
- Embedded Software Synthesis that is used into the ESL design flow
COMPLEX Related Special Session & Demo
A special session was held on Sunday, June 3 regarding COMPLEX related topics and presented by COMPLEX Consortia members:

- Achim Rettberg, University of Oldenburg,
- William Fornaciari, PoliMi,
- Franco Fummi, University of Verona.

COMPLEX related papers:

- *Design Space Exploration*, Vittorio Zaccaria, Politecnico di Milano – PoliMi

Furthermore, discussions and other relevant COMPLEX activities were held each day of the conference during the poster presentation.
2.1.9 ISCUG 2013 – India SystemC User Group Conference

- **Tutorial Day:** 14th April, 2013 (Sunday)
- **Conference Day:** 15th April, 2013 (Monday)
- **Venue:** Hotel Radisson, Noida, India
- **Audience:** about 150 participants
- **Website:** [http://iscug.in/ISCUG-2013](http://iscug.in/ISCUG-2013)

**About the conference**

The Indian SystemC User's Group (ISCUG) organization aims to accelerate the adoption of SystemC as the open source standard for ESL design. We provide a platform to share the knowledge, experiences and best practices about SystemC usage.

We organize an annual conference which provides a platform for the SystemC beginners, the SystemC experts, ESL managers and the ESL vendors to share their knowledge, experiences & best practices about SystemC usage. The event is also useful for the following target audience.

- Electronics Systems developers who want to explore SystemC based ESL methodologies
- System on Chip (SoC) Architects: Working on architectural exploration for power & performance optimization
- Embedded software developers who want to use Virtual Platforms
- Chip design engineers who want to explore SystemC based chip design at the abstraction above RTL
- Chip verification engineers who want to explore SystemC based verification methodologies

**COMPLEX contribution**

As there is a vibrant and technically excellent SystemC community in India and the event had a strong industrial focus, it has been a very good opportunity to present some of the latest COMPLEX project results.

Although the India SystemC User’s Group conference strictly speaking happened after the end of the COMPLEX project, two COMPLEX-related presentations have been given at ISCUG’2013 that are worth mentioning.

Invited keynote talk:

**Beyond algorithms and performance: Modelling extra-functional properties in SystemC**

Philipp A. Hartmann (OFFIS)

SystemC and TLM-2.0 based ESL methodologies are widely used for early application, platform, and performance analysis already. But the consideration of an embedded device's power consumption and its management is increasingly important nowadays, not only for mobile devices. Currently, it is not equally easily possible to integrate such extra-functional information at electronic system-level.

In this talk, the design challenges of today's heterogeneous HW/SW systems regarding power and complexity, both for platform vendors as well as system integrators are discussed. Existing and new approaches for system-level timing and power estimation techniques, as well as their efficient integration into SystemC/TLM virtual prototypes are presented. To enable interoperability beyond timing and functionality, the need for future standardization efforts in the area of extra-functional properties is motivated.
The main focus of the keynote presentation has been to provide a view on the need for modeling support of extra-functional properties in the SystemC ecosystem. Since there are a lot of open issues to overcome, before a full standard in this area could be established, a roadmap for smaller, incremental steps this long-term goal has been given.

Tutorial presentation:
**Leveraging Non-Intrusive TLM-2.0 Transaction Introspection for Power-Aware Virtual Prototyping**
Philipp A. Hartmann (OFFIS)

Integrating third-party TLM-2.0 components into custom system models frequently requires the definition of wrappers to adapt the particular behaviour and analysis/tracing capabilities of such a component to the concrete needs of the overall platform. In this tutorial, a simple yet powerful mechanism for introspection and augmentation is presented, greatly reducing the amount of required boiler-plate code in such cases. Custom convenience sockets for transaction introspection and forwarding are introduced and required implementation techniques are discussed. In the second part, this augmentation mechanism is used to externally add power information in terms of a state-machine based abstraction to a pre-existing TLM-2.0 system.

During the tutorial session, a practically oriented introduction to the COMPLEX modeling technology has been given. A lot of interest also on the open-source implementation has been expressed by the audience.

Figure 2 ISCUG’2013 tutorial; 14th April 2013, Noida, India.
2.2 Conference Papers & Publications

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<tr>
<td>COMPLEX deliverable</td>
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<td>deliverable</td>
<td>Dissemination Activities. Number COMPLEX/ECSI/R/D5.2.2/1.0, COMPLEX project deliverable, May 2012. [url]</td>
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<td><em>System Specification and Design</em></td>
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<td><strong>COMPLEX deliverable</strong></td>
<td>Carlo Brandolese, Gianluca Palermo, William Fornaciari, H’ector Posadas, Fernando Herrera, Pablo Peñil, Eugenio Villar, Francisco Ferrero, Ra’ul Valencia and Bart Vanthournout. <em>Final report on embedded software estimation and model generation</em>. Number COMPLEX/PoliMi/R/D2.2.2/1.0, COMPLEX project deliverable, January 2012. [url]</td>
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<td><strong>COMPLEX deliverable</strong></td>
<td>Sara Bocchio, Philipp A Hartmann, Daniel Lorenz and Davide Quaglia. <em>Final report and tools on platform IP components estimation and model generation</em>. Number COMPLEX/ST-I/P/D2.3.2/1.1, COMPLEX project deliverable, May 2012.</td>
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<td><strong>COMPLEX deliverable</strong></td>
<td>Kai Hylla, Pablo Gonz’alez, Pablo S’anchez and Fernando Herrera. <em>Final report on custom hardware estimation and model generation</em>. Number COMPLEX/OFFIS/P/D2.4.2/1.0, COMPLEX project deliverable, January 2012. [url]</td>
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<td><strong>COMPLEX deliverable</strong></td>
<td>Chantal Ykman-Couvreur, Sven Rosinger, Kai Hylla and Gianluca Palermo. <em>Intermediate report on run-time management</em>. Number COMPLEX/IMEC/R/D3.5.2/1.3, COMPLEX project deliverable, December 2011. [url]</td>
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<td>COMPLEX deliverable</td>
<td>Fernando Herrera, Pablo Penñil, Eugenio Villar, Francisco Ferrero, Raul Valencia, Luciano Lavagno and Davide Quaglia. <em>SystemC generation tools from MARTE and Stateflow.</em> Number COMPLEX/UC/P/D2.1.2/1.0, COMPLEX project deliverable, June 2011. [url]</td>
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<td>uPM²SoC</td>
<td>Kim Grüttnner, Kai Hylla, Sven Rosinger, Philipp A Hartmann and</td>
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### COMPLEX deliverable

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<td>Chantal Ykman-Couvreur, Sven Rosinger, Kai Hylla and Gianluca Palermo.</td>
<td>Preliminary report on run-time management.</td>
<td>Number COMPLEX/IMEC/R/D3.5.1/1.0, COMPLEX project deliverable, March 2011. [url]</td>
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<td>Adam Morawiec</td>
<td>Preliminary Report on Standardization and Dissemination Activities.</td>
<td>Number COMPLEX/ECSI/R/D5.2.1/1.0, COMPLEX project deliverable, January 2011. [url]</td>
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<td>MTVcon 2010</td>
<td>Nicola Bombieri, Franco Fummi, Valerio Guarnieri, Graziano Pravadelli</td>
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<td>EWDTS 2010</td>
<td>Redesign and Verification of RTL IPs through RTL-to-TLM Abstraction and TLM Synthesis</td>
<td>Nicola Bombieri, Diego Forrini, Franco Fummi, Laurenzi Matteo and Sara Vinco.</td>
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<td>COMPLEX deliverable</td>
<td>Definition of application, stimuli and platform specification, and definition of tool interfaces.</td>
<td>Gianluca Palermo, Carlo Brandolese, Francisco Ferrero, Fernando Herrera, Gunnar Schomaker, Claus Brunzema, Kim Grüttnner, Kai Hylla, Bart Vanthournout, Davide Quaglia, Luciano Lavagno, Massimo Poncino, Emanuel Vaumorin, Chantal Couvreur and Saif Ali Butt.</td>
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<td>Adam Morawiec. Plan for Dissemination to the Public. Number COMPLEX/ECSI/R/D5.3.1/1.0, COMPLEX project deliverable, May 2010. [url]</td>
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2.3 Organisation of Open Workshops

The following workshops were organized at the European Level by ECSI inviting partners to present and disseminate specific project results to a broad group of researchers, system designers and managers. These workshops are focused on potential stakeholders on specific technology or standardization bodies.

2.3.1 2nd Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures

**Website:** [http://conferences.microlab.ntua.gr/parma2011/](http://conferences.microlab.ntua.gr/parma2011/)

**Date & Place:** Lake Como, Italy, February 23, 2011

(Co-located with ARCS 2011 - Architecture of Computing Systems)

**Organization:** POLIMI

**Description:**
The current trend towards many-core architecture requires a global rethinking of software and hardware design approaches. The PARMA workshop focuses on parallel programming models, design space exploration and run-time resource management techniques to exploit the features of many-core processor architectures. The PARMA workshop is composed of three main sessions:

- **S1:** Programming models and languages, compilers and virtualization techniques
- **S2:** Runtime management, power management and memory management
- **S3:** Design space exploration and many-core architecture customization

**COMPLEX activities:**
This workshop organized by POLIMI has the objective to create networking around some of the project activities and to spread-out the knowledge especially focused on design space exploration, programmability, software optimization and estimation and run-time management issues for embedded systems. In this workshop POLIMI will present research and development activities related to COMPLEX.

**Organizing Committee**

**Workshop General Co-Chairs:**

Dimitrios Soudris, National Technical University of Athens, Greece

Giovanni Agosta, Politecnico di Milano, Italy

**Session Chairs:**

S1: Torsten Kempf, ISS-RWTH Aachen University, Germany

S2: Gianluca Palermo, Politecnico di Milano, Italy

S3: Benno Stabernack, Heinrich Hertz Institute, Fraunhofer Institute, Germany

**Publicity Chair:**

Arindam Mallik, IMEC

**Publication Chair:**

Carlo Galuzzi, Delft University of Technology
2.3.2 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications (DEPCP'2011)


**Date & Place:** March 18, 2011, Grenoble, France (co-located with DATE'11, Friday Workshop W3)

**Organization:** POLIMI

**Description:**
The future of embedded computing is shifting to multi/many-core designs to boost performance due to the unacceptable power consumption and operating temperature increase of fast single-core CPU's. Hence embedded system designers are increasingly faced with the following new big challenges: the support for a variety of concurrent applications, and the platform heterogeneity. These challenges lead to the following significant issues:

- How can we write applications that exploit the underlying (parallel) architecture, without burdening the application designer?
- What does the application designer really need to know of the underlying architecture?
- What tools are needed to efficiently map applications and what part of the process should be automated?
- How should we design the underlying architectures?

This workshop brings together researchers actively working on architectures, design tools, and applications for embedded parallel computing platforms to address these questions and related issues.

**Topic Areas:**
The workshop focused on three main sessions:

- **Architectures:** on the most relevant problems arising during the design exploration and optimization of many/multi core architectures.
- **Design tools:** on the state-of-the-art of tool development, showing where we are now and the directions we need to move in.
- **Applications:** on the analysis, development, modification and integration of applications with respect to parallel computing platforms.

This workshop organized by POLIMI with the support also of IMEC has the objective to create networking around some of the project activities and to spread-out the knowledge especially focused on design space exploration, programmability, software optimization and estimation and run-time management issues for embedded systems. In this workshop POLIMI will present research and development activities related to COMPLEX.

**COMPLEX related posters:**

- *Audio Driven Video Surveillance System using COMPLEX design flow.*
  Fabien Colas-Bigey (Thales), Sara Boccio (ST-I), Chantal Ykman-Couvreur (IMEC), Gianluca Palermo (PoliMi), Philipp A. Hartmann (OFFIS)

- *Using the COMPLEX Design Flow for Space Domain Applications*
  Francisco Ferrero (GMV), Kim Grüttn (OFFIS), Fernando Herrera (UC), Gianluca Palermo (PoliMi), Bart Vanthournout (SNPS), Emmanuel Vaumorin (MDS)

  Philipp A. Hartmann, Philipp Ittershagen, Kim Grüttn, Frank Oppenheimer (OFFIS), Achim Rettberg, (University of Oldenburg)
Organization:
General Co-Chairs: Cristina Silvano and Giovanni Agosta, Politecnico di Milano, Italy
Architectures Session Chair: Maurizio Palesi, KORE University, Italy
Design Tools Session Chair: Chantal Ykman-Couvreur, IMEC, Belgium
Applications Session Chair: Diana Göhringer, Fraunhofer IOSB, Germany
Poster Session Chair: Michael Hübner, Karlsruhe Institute of Technology, Germany
Panel Session Co-Chairs: Jürgen Becker and Michael Hübner, Karlsruhe Inst. of Technology, Germany
Web and Posters Submission Chair: Fabrizio Castro, Politecnico di Milano, Italy
Publicity Chair: Maurizio Palesi, KORE University, Italy

2.3.3 Early Timing and Power Information of Complex SoC Designs using Augmented Virtual Platforms

Web site: http://complex.offis.de/news/82-date2011#exhibition-theatre-session
Date & Place: March 17, 2011, Exhibition Theatre at DATE
Organization: OFFIS
Organizer: Kim Grüttnner (OFFIS)

Rationale and Abstract:
Consideration of an embedded system’s timing behavior and power consumption at system-level is an ambitious task. Sophisticated tools and techniques exist for power and timing estimations of individual components such as custom hard and software as well as IP components. But prediction of the composed system behavior can hardly be made.

In this session we present the concept of an ESL framework for timing and power aware rapid virtual system prototyping of embedded HW/SW systems. Our proposed flow combines system-level timing and power estimation techniques available in commercial tools with platform-based rapid prototyping. Our proposal aims at the generation of executable virtual prototypes from a functional C/C++ specification. These prototypes are enriched by static and dynamic power values as well as execution times. They allow a trade-off between different platforms, mapping alternatives, and optimization techniques, based on domain-specific workload scenarios.

Presentations:
- The COMPLEX ESL Framework for Timing and Power Aware Rapid Prototyping of HW/SW Systems
  Kim Grüttnner - OFFIS
- Using Virtual Platforms for Energy Efficient SW-Design
  Bart Vanthournout - Synopsys
- Automatic Abstraction of RTL IPs into Equivalent TLM Descriptions for Platform Simulation
  Franco Fummi - EDALab
- Choosing IP-XACT IEEE 1685 standard as a unified description for timing and power performance estimations in virtual platforms
  Emmanuel Vaumorin – Magillem Design Services
2.3.4 M-BED’2011, the 2nd Workshop on Model Based Engineering for Embedded Systems Design

Web site: http://www.ecsi.org/m-bed

Date & Place: March 18, 2011, Grenoble, France (co-located with DATE)

Organization: ECSI

Description:
The application of model-based engineering (MBE) methods for software and systems development in industry is increasing. Moreover, the integration of component-based approaches with MBE has further accelerated its adoption along with providing a basis for a sounder theoretical underpinning.

The focus of this workshop is on the use of MBE for embedded systems development (e.g. in the industrial transport sector for applications such as railway systems, automotive, aerospace, and related domains). In this context, special focus is given to MARTE, the UML profile for Modelling and Analysis of Real-Time and Embedded systems, which has proven successful in a number of projects. In particular, the program concentrates on the following topics:

- The infrastructure that supports MBE, that is, the requisite languages, tools, and standards, as well as the combination of design and V&V activities, and the diverse engineering disciplines involved in embedded system design.
- Process and methodology related issues, such as guidelines for deciding when and how to use domain-specific languages, appropriate integration of tools, and advanced methods to assist on architecture exploration subjected to multiple non functional constraints.
- Experience with applying MARTE and suggestions of improvements to this standard.

The aim of the workshop is to bring together researchers as well as system designers and tool developers from both industry and academia to discuss applications of model-based engineering in general and MARTE usage in particular. A significant portion of time will be reserved for discussion.

Complementing the accepted paper presentations will be several invited presentations by members of the MARTE standardization task force, specialists participating in relevant European projects, and representatives of MBE tool vendors. The one-day workshop is organized in multiple sessions, each focusing on a particular topic. Rather than have questions at the end of each presentation, all discussion will be conducted at the end of the session, with all presenters in the session responding as a group to questions of the session moderator as well as other attendees.

Organizers:
Pierre Boulet, Univ. Lille, FR
Daniela Cancila, Sherpa Engineering, FR
Sébastien Gérard, CEA-LIST, FR
Adam Morawiec, ECSI, FR
Chokri Mraihda, CEA-LIST, FR
Laurent Rioux, Thales RT, FR
Bran Selic, Malina Software Corp., CA
In this workshop some preliminary results from UC side will be presented regarding the IP-XACT generation from UML/MARTE. Specifically, the following paper will be presented:

F. Herrera, E. Villar.

### 2.3.5 Workshop on Micro Power Management for Macro Systems on Chip (uPM2SoC)

**Web site:** [http://www.ece.cmu.edu/~dianam/uPM2SoC10/](http://www.ece.cmu.edu/~dianam/uPM2SoC10/)

**Date & Place:** March 18, 2011, Grenoble, France (co-located with DATE)

**Organizers:**

Technical program:
Diana Marculescu, Carnegie Mellon University
Suzanne Lesecq, CEA-LETI Minatec

Invited talks:
Diego Puschini, CEA-LETI Minatec

Panel session:
Radu Marculescu, Carnegie Mellon University

**Description:**
Increased integration of hundreds of processing cores on the same silicon substrate has allowed the concurrent execution of multiple applications on a chip, but at the cost of significant increase in on-chip power consumption. On-chip power management has therefore become a critical component of every step in the many-core design flow, from physical design all the way up to micro-architecture and system-level design. While dynamic power management has been extensively studied for the case of single-core systems, many-core systems present additional challenges that require maintaining appropriate performance levels for applications running on the system both in the context of turning on/off cores and using selectively power states, or in the context of using Dynamic Voltage Frequency Scaling (DVFS) for enabling a certain performance level at a minimum power. Furthermore, enabling power management at macroscale – for hundreds or thousands of on-chip resources – while relying on capabilities developed at microscale – specifically, technology and device-level knobs – becomes an essential for effective power control.

This workshop addresses this need by targeting emerging topics in power management and control of large scale many-core systems, such as scalability, distributed vs. centralized vs. hybrid approaches, as well as technology-driven challenges that need to be considered for providing a truly power-aware solution, such as static and dynamic variations and reliability, as well as limits for control strategies for technologies 22nm and beyond.

**COMPLEX related poster:**

  Kim Grüttner, Kai Hylla, Sven Rosinger, Philipp A. Hartmann, Wolfgang Nebel, OFFIS.
2.3.6 Embedded Software Development on Virtual Platforms – Ready for Prime Time?

Date & Place: February 28, 2012, Nuremberg, Germany (at Embedded World)
Organization: ECSI, OFFIS

Organizers:
Adam Morawiec, ECSI, France
Frank Oppenheimer, OFFIS, Germany

Motivation:
Embedded software development process and methodologies aims today mainly at simple single-core platforms. Due to power constraints today’s high performance platforms are dominated by multi-core and heterogeneous architectures. To efficiently exploit these platforms in the software development process we need to carefully consider the platform artefacts, features and strengths.

Current software development process is not efficient anymore because of:
- Long overall development time of software starting late after the underlying hardware platform is available
- Difficult debugging, testing and validation of software on complex hardware platforms
- Optimized usage of available resources (hardware, low-level software, …)
- Cost of optimization, re-spins, bug fixing in both software and hardware

Virtual Platforms offer a viable and powerful solution to the above weaknesses.

Description:
Development and integration of embedded software executing on a hardware platform is increasingly becoming a key factor in product differentiations well as in its final market success or failure. Not only does the software development process determine the overall product functionality, it also significantly influences its entire development time. If the software is finished too late then the entire product can fail.

In addition software complexity is growing and consumes significant development and verification time. Add to this the trend towards multi-core architectures today, which makes them challenging to analyze and debug, and it should come as no surprise that recent studies show that software development effort already surpasses the effort spent on hardware for a typical 90nm SoC design. Furthermore, software becomes an integral part of any system verification concept, as only the combination of hardware and software allows verifying system functionality.
With an ever growing system complexity the industry needs to apply new concepts, paradigms and methods for embedded software development and hardware/software system validation that will be able to tackle with the problems of quality and correctness, providing significant gain in the design productivity and shorten time to market.

It is the belief that such a new way of development will be based on **embedded software development on virtual platforms**. The concept of system virtualization has been around for almost a decade, during which time the industry started to learn how to build and apply these technologies. Topics of controversy have been the necessary accuracy vs. possible simulation performance, the need for a system-level IP eco system, and the move from tool-specific simulation paradigms towards public standards.

This workshop will cover the state-of-the-art of embedded software development on virtual platforms. This includes technologies and tool environments for building, executing and distributing virtual platforms. It will address existing and upcoming industry standards. Significant room will be given to cover user experience, both from those building virtual platforms, as well as from those deploying virtual platforms for embedded software development, or software-driven system validation.

Lessons learned, problems solved, remaining issues will be shared with the participants.

**Target Audience:**
- Embedded software developers: application, hardware dependent software, and driver developers
- Embedded system developers
- Software verification engineers
- Virtual platform developers

**COMPLEX related presentations:**
*Software Simulation Technologies in Virtual Platforms*
Eugenio Villar, University of Cantabria, Spain

*The COMPLEX Virtual Platform Design Approach for Performance and Energy Efficient Embedded Systems: A European Research Perspective*
Frank Oppenheimer, OFFIS, Germany

*COBRA, Using a Virtual Platform for the Design of a Programmable Wireless Baseband System*
Jeroen Declerck, IMEC, Belgium

**Virtual Platform Eco-System: Tools, IPs and Services Demonstrations:**
- EDALab
- Magillem
2.3.7 Quo Vadis, Virtual Platforms? Challenges and Solutions for Today and Tomorrow (QVVP12)

Website:  http://qvvp12.offis.de

Date & Place:  March 16, 2012, Dresden, Germany (co-located with DATE)

Organizers:
Rainer Leupers, RWTH Aachen University, DE
Christian Haubelt, University of Rostock, DE
Achim Rettberg, Carl von Ossietzky University Oldenburg, DE
Kim Grüttner, OFFIS – Institute for Information Technology, DE

Rationale and Abstract

Nowadays, the deployment of Virtual Platform models is an industry-proven technique in a wide variety of design tasks from pre-silicon software development to performance analysis and exploration. With the increasing complexity, both in terms of the applications and the target platforms (e.g. increasing number of cores, more complex memory hierarchies), the Virtual Platform per se is not an answer to all of today’s design challenges. But by adding further abstraction to the models, an increasing need for automated mapping, refinement, and model transformations is needed. Formal, static, and dynamic analysis methods are increasingly dependent on platform details, requiring traceability during all design phases.

This workshop aims to bring together developers, researchers, and managers from industry and academia to develop a perspective for the future use of Virtual Platforms by exchanging knowledge about current and future requirements and their possible solutions. The workshop will also provide some space for the provision of state of the art and tangible results and session on tool demos.

Questions addressed during the workshop are:
- How to efficiently generate a Virtual Platform for new applications and HW platforms?
- How to close the implementation/refinement gap?
- Which properties of a real system can be captured?
- What are the requirements for future Virtual Platforms?
- How can Virtual Platforms support the development of future real-time applications for MPSoCs?

In this workshop, different points of view have been discussed by
- potential users of Virtual Platforms from different domains
- tool vendors already offering Virtual Platform tools and modeling techniques, and
- academic research institutes from around the world showing recent progress in Virtual Platform synthesis and core technologies.

Who attended?

This Friday Workshop gave an extensive overview on research directions around Virtual Platforms, covering system and Virtual Platform synthesis, Timing and Power modeling using Virtual Platforms, and support for the development of hard real-time applications on multi-core Platforms. The workshop has been visited by researchers and professionals who wanted to get an insight in future design methodologies as well as managers who wanted to acquire a basic knowledge on the usage of Virtual Platforms.
COMPLEX related presentations:
Task Modeling and HW/SW partitioning for System Performance Optimization
Tim Kogel – Synopsys, DE

High-Level Synthesis, TLM Power State Machines, and advanced tracing for Virtual Platforms
Philipp A. Hartmann – OFFIS – Institute for Information Technology, DE

2.3.8 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications (DEPCP’2012)
Web site: http://conferenze.dei.polimi.it/depcp/
Date & Place: March 16, 2012, Dresden, Germany (co-located with DATE’12)
Organization: POLIMI

Description:
Embedded computing is shifting to multi/many-core designs to boost performance due to unacceptable power consumption and operating temperature increase of fast single-core CPU's. Hence, embedded system designers are increasingly faced with several big challenges, namely: the support for a variety of concurrent applications, and the platform heterogeneity. These challenges lead to the following significant design issues:

- How can applications that exploit the underlying (parallel) architecture be written without burdening the application designer?
- What does the application designer really need to know of the underlying architecture?
- What tools are needed to efficiently map applications and what part of the mapping process should/could be automated?
- How should we design and optimize the underlying architectures?

This workshop brings together researchers and practitioners actively working on architectures, design tools, and applications for embedded parallel computing platforms to address these questions and related issues.

Topic Areas:
The workshop will have three main topic areas:

- **Architectures**: on the most relevant problems arising during the design exploration and optimization of many/multi core architectures.
- **Design tools**: on the state-of-the-art of tool development, showing where we are now and the directions we need to move in.
- **Applications**: on the analysis, development, modification and integration of applications with respect to parallel computing platforms.

COMPLEX related posters:
- **Energy-aware run-time management in video surveillance systems**
  Laurent San (Thales), Sara Bocchio (ST-I), Chantal Ykman-Couvreur (IMEC), Gianluca Palermo (PoliMi), Philipp A. Hartmann (OFFIS)
Organization:
General Co-Chairs: Cristina Silvano and Giovanni Agosta, Politecnico di Milano, Italy, and Joao Cardoso, Universidade do Porto, Portugal
Architectures Poster Session Chair: Maurizio Palesi, KORE University, Italy
Design Tools Session Chair: Chantal Ykman-Couvreur, IMEC, Belgium
Applications Session Chair: Diana Göhringer, Fraunhofer IOSB, Germany
Posters Submission Chair: Dimitris Mpekiaris, National Technical University of Athens, Greece
Publicity Chair: Maurizio Palesi, KORE University, Italy

2.3.9 Embedded Software Development on Virtual Platforms – Are We Ready For Industrial Deployment?

Web site:
Date & Location: February 26, 2013 - Nuremberg, Germany
Organizer: ECSI, OFFIS

Embedded Software Development on Virtual Platforms – Are We Ready For Industrial Deployment?

at Embedded World!

February 26, 2013
Nuremberg, Germany

Organizers:
Adam Morawiec, ECSI
Frank Oppenheimer, OFFIS

Motivation:
Embedded software development process and methodologies aims today mainly at simple single-core platforms and is detached from performance characteristics of the underlying hardware and hardware-dependent software. Due to power and performance constraints today’s most advanced platforms are dominated by multi-core and heterogeneous architectures. To efficiently exploit these platforms in the software development process we need to carefully consider the platform artefacts, performances, characteristics, features and strengths.

Current software development process is not efficient anymore because of:
- Long overall development time of software starting late after the hardware platform is available
- Difficult debugging, testing and validation of software on complex hardware platforms
- Optimized usage of available resources (hardware, low-level software, …)
- Cost of optimization, re-spins, bug fixing in both software and hardware

Virtual Platforms offered a viable and powerful solution to the above weaknesses.
Description:
This workshop covered the state-of-the-art of embedded software development on virtual platforms. This includes technologies and tool environments for building, executing and distributing virtual platforms. It had addressed existing and upcoming industry standards. Significant room has been given to cover user experience, both from those building virtual platforms, as well as from those deploying virtual platforms for embedded software development, or software-driven system validation.

Lessons learned, problems solved, remaining issues were shared with the participants.

**COMPLEX related presentations:**
- **Introduction: Embracing Software Development Processes**
  Eugenio Villar, University of Cantabria, Spain
- **Performance and Energy Modeling and Analysis in COMPLEX Virtual Platform**
  Frank Oppenheimer, OFFIS, Germany
- **Platform Design Environment / Platform Generation Tools**
  Andreas Hoffmann, Synopsys, Germany

**Target Audience:**
- Embedded software developers: application, hardware dependent software, and driver developers
- Embedded system developers
- Software verification engineers
- Virtual platform developers

Figure 3 Virtual Platform workshop at Embedded World.
2.3.10 Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications (DEPCP'2013)

Website: http://conferenze.dei.polimi.it/depcp/
Date & Place: March 22, 2013, Grenoble, France (co-located with DATE'13)
Organization: POLIMI

Description:
Embedded computing is shifting to multi/many-core designs to boost performance due to unacceptable power consumption and operating temperature increase of fast single-core CPU's. Hence, embedded system designers are increasingly faced with several big challenges, namely: the support for a variety of concurrent applications, and the platform heterogeneity. These challenges lead to the following significant design issues:

- How can applications that exploit the underlying (parallel) architecture be written without burdening the application designer?
- What does the application designer really need to know of the underlying architecture?
- What tools are needed to efficiently map applications and what part of the mapping process should/could be automated?
- How should we design and optimize the underlying architectures?

This workshop brings together researchers and practitioners actively working on architectures, design tools, and applications for embedded parallel computing platforms to address these questions and related issues.

Topic Areas:
The workshop will have three main topic areas:

- **Architectures**: on the most relevant problems arising during the design exploration and optimization of many/multi core architectures.
- **Design tools**: on the state-of-the-art of tool development, showing where we are now and the directions we need to move in.
- **Applications**: on the analysis, development, modification and integration of applications with respect to parallel computing platforms.

Organizers:
- João Cardoso (Universidade do Porto Portugal)-
- Cristina Silvano (Politecnico di Milano, Italy)
- Dimitrios Soudris (National Technical University of Athens, Greece)
- Architectures Posters Session Chair: Maurizio Palesi (KORE University, Italy)
- Design Tools Posters Session Chair: Chantal Ykman-Couvreur (IMEC) Applications Posters Session Chair: Giovanni Agosta (Politecnico di Milano)
- Panel Session Chair: Georgi Gaydadjiev (Chalmers University of Technology)
- Web and Posters Chair: Sotirios Xydis (Politecnico di Milano, Italy)
COMPLEX Related Activities:

Panel on: "Lessons Learnt from 2PARMA, COMPLEX, ERA, FASTER, MADNESS, PARAPHRASE, REFLECT, SMECY and TERAFLUX European Projects"

Panel Organizer and Moderator: Georgi Gaydadjiev, Chalmers University of Technology:

- Panelists: William Fornaciari (Politecnico di Milano)
- Philipp A. Hartmann (OFFIS)
- Stephan Wong (TU Delft)
- Dionisios Pnevmatikatos (Technical University of Crete)
- Luigi Raffo (Università di Cagliari)
- Kevin Hammond (Univ. Of St. Andrews)
- Zlatko Petrov (Honeywell)
- Francois Pacull (CEA)
- Roberto Giorgi (Università di Siena)

Description:
This panel is organized to present and discuss final outcomes and lessons learnt from the following on-going EU funded projects: 2PARMA (PARallel PARadigms and Run-time MAnagement techniques for Many-core Architectures), COMPLEX (COdesign and power Management in PLatform-based design space Exploration), DeSyRe (DeSyRe: on-Demand System Reliability), ERA (Embedded Reconfigurable Architecture), FASTER (Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration), MADNESS (Methods for predictAble Design of heterogeneous Embedded Systems with adaptivity and reliability Support), PARAPHRASE (Parallel Patterns for Adaptive Heterogeneous Multicore Systems) REFLECT (Rendering FPGAs to Multi-Core Embedded Computing), SMECY (Smart Multicore Embedded Systems) and TERAFLUX (Exploiting Dataflow Parallelism in Teradevice Parallelism).

COMPLEX related posters:
- Design Space Exploration and Analysis Of Compiler Transformation in VLIW Processors. A. Ashouri, V. Zaccaria, S. Xydis, G. Palermo and C. Silvano (PoliMi)
- Energy-aware run-time management in video surveillance systems Laurent San (Thales), Chantal Ykman-Couvreur (IMEC), Gianluca Palermo (PoliMi)
2.3.11 5th Workshop on: Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO)

Website: http://www.hipeac.net/rapido/2013

Date & Place: January 21, 2013 - Berlin, Germany (co-located with HiPEAC 13)

Organization: POLIMI - THALES

Description:
The focus of the RAPIDO’13 Workshop is on methods and tools for rapid simulation and performance evaluation in embedded and high performance systems design. Given continuous advances in chip technology, it is to be expected that future-generation processors will integrate numerous units on a single die, including multiple processor cores, multiple levels of (shared/private) caches or memories, and multiple dedicated accelerators, which will be glued together through a network on-chip (NoC).

In the embedded domain, the Intellectual Property (IP) based design approach is one of the most popular solutions to overcome this design challenge by relying on parameterized, pre-designed and pre-verified IP cores. Simulators are then used to explore the huge design space of interconnected IP cores for finding the optimal design for a given application domain. In the general-purpose computing domain, the time-to-market is typically longer, the design is typically not limited to interconnecting pre-existing IP cores, however, the design should be optimized for a broader set of applications. In both the embedded and the general-purpose domains, searching the huge design space during the design process is done through Design Space Exploration (DSE). DSE involves a number of key technologies such as modeling, simulation, prototyping, heuristic searching, etc. which have to cooperate in order to make the exploration effective, i.e., to obtain a final design with an optimal performance/power/cost/reliability ratio for the application domain of interest without compromising the time-to-market.

Although DSE is essential to both embedded and general-purpose processor design, both communities are largely unaware of each other’s work and progress. The purpose of this workshop therefore is to bridge this gap, and bring together researchers and practitioners from both communities to learn and discuss recent progress, and stimulate the interaction between both communities by exchanging ideas and sharing experiences. The workshop should provide a forum for brainstorming and road-mapping future DSE technologies for both the embedded and general-purpose domains.

Organizers:
- Daniel Gracia Pérez, Thales Research and Technology France, France
- Morteza Biglari-Abhari, University of Auckland, New Zealand
- Gianluca Palermo, Politecnico di Milano, Italy
- Daniel Chillet, Université de Rennes 1, France

COMPLEX Related Activities:

- Poster and Demo about MOST DSE Tool: (PolIMI)
2.4 Specific Focused Dissemination Actions

2.4.1 HIFSuite Dissemination
EDALab is particularly promoting HIFSuite, upon which some COMPLEX tools rely, through a massive marketing campaign consisting of the following events:

- EDALab hosted by the UNIVR University booth at DATE 2010
- Industrial Practice Session of the IEEE High-Level Design Validation and Test Workshop (HLDVT) 2010
- EDALab booth at DATE 2011
- EDALab booth at DAC 2011
- EDALab booth at Embedded World 2012
- EDALab booth at Embedded World 2013

A new ad hoc web site (http://hifsuite.edalab.it) has been set up at the beginning of March 2010. Regarding the commercial distribution, a demo version has been made freely available on the HIFSuite website to let potential users play with small designs.

During the period of COMPLEX project, HIFSuite has become a more solid industrial product and some project achievements (e.g., abstraction tool named A2T) have increased the added value offered to the customers.

A plan for periodic release of new versions has been setup with two different distributions:

- Commercial distribution with the most stable and tested functionalities, i.e., HDL translation and abstraction.
- Internal distribution with the features of the commercial distribution and more recent advances; it is freely available to COMPLEX partners, contributors and beta-testers.

At Embedded World 2013 an industrial paper was presented to describe the HDL manipulation methodologies. The paper is now available on the HIFSuite website.

Google AdWords service was adopted to create target-specific campaigns. A mailing campaign has been launched to promote HIFSuite among research groups all over the world.

2.4.2 SCNSL Dissemination
An open source project has been created on SourceForge website http://scnsl.sourceforge.net to increase sharing of ideas and cooperative development.

2.4.3 Synopsys Webinar and Users’ Group Meetings
Synopsys has been promoting the power modeling technology in an online webinar titled “Low Power Video Processing or the Mobile SoC: How Analysis of HW-SW partitioning gets the most from Embedded GPU’s”. In this webinar the overall architecture design solution from Synopsys was described with specific attention to the new power modeling and analysis features. This event was broadcast on October 18, 2012 with over 70 live registrations.

The power modeling methodology will also be presented at the Synopsys user group meetings (SNUG) in Silicon Valley and Munich.
2.5 Project e-Platform

The project web portal provides access to the project results at three different levels:

- Public level: includes public information, presentations and open results.
- Restricted level: includes information like deliverables and presentations for project reviews, accessible only to project members and European Commission (EC) reviewers and/or jointly agreed additional companies out of the project.
- Confidential level: contains all partial and final results, working documents, presentations and articles.

The project web portal can be found at [https://complex.offis.de/](https://complex.offis.de/). This website will be continuously maintained by OFFIS beyond the project’s lifetime. Additional resources related to the evolution of the COMPLEX results in the future will be referenced from there.

Additionally the project provides access to open source repositories for the open source tools developed within the project. Instead of relying on a custom infrastructure, the results have been (or will be made) available via standard collaboration platforms like GitHub ([http://github.com/](http://github.com/)) or SourceForge ([http://sf.net/](http://sf.net/)). Links to the tool’s pages at these platforms will be put prominently on the main project website.

Overall, the project website has gained international visibility. Over the project’s run-time, more than 5,000 unique visitors and nearly 20,000 page views have been attracted. A detailed analysis can be found in the Annex of this report.

2.6 E-mailing

The announcements of events and availability of open results was largely disseminated on ECSI’s email lists for system design/embedded systems (currently containing more than 22000 entries) and other companies’ lists.
3 Standardization Activities

This section describes the standardization bodies, tasks and responsibilities necessary to coordinate all standardization activities of the project in a consistent and coherent way. These activities encompass the following sub-activities:

- Elaboration of standard proposals (definitions, recommended practices, requirements, example models, etc.)
- Internal review of proposals, including the nomination of reviewers, planning of review meetings and control of received comments.
- Participation in relevant Working Groups closely related with standardization bodies.
- Interaction between the project and standardization bodies.

3.1 Standardization Bodies

The following standardization bodies are identified in the context of the COMPLEX project:

3.1.1 Accellera Systems Initiative – SystemC (formerly OSCI)

COMPLEX provides inputs to the standardisation of SystemC/TLM. Project partners have directly participated in relevant Accellera Systems Initiative SystemC working groups (formerly OSCI working groups), namely the SystemC Language Working Group (LWG), SystemC Transaction-Level Modelling Working Group (TLMWG), and the SystemC Control Configuration and Introspection Working Group (CCIWG).


The COMPLEX work on SystemC has concerned also the IEEE1666 standardization.

3.1.2 Accellera System Initiative – IP-XACT

COMPLEX has provided inputs to the IP-XACT standardization working group of Accellera. Feedback and improvements proposals for existing versions of the standard (e.g. IP-XACT 1.4 and 1.5) as well as requirements for upcoming versions of IP-XACT have been provided. Project partners have directly participated in relevant IP-XACT Working Groups: Extensions, Registers.


Below a typical IP-XACT based design flow is presented.
Among the current and future topics of evolution, Accellera enumerates specific extensions (new area) development for:

- Power analysis (IP Power model, Power domains)
- Early-prototyping (Area / Timing / Power expressions)
- Verification and Debug (Testbench, systemVerilog)
- AMS where power domain has a privileged priority.

### 3.1.3 OMG UML

COMPLEX has provided inputs to the OMG for UML profile MARTE standardisation and evolution. Project partners have been involved in the definition of the COMPLEX design entry based on the UML/MARTE modelling language analyzed current MARTE specification. During the use case implementation they have provided feedback to the OMG organization in relevant aspects related to the design of Real-Time Embedded Systems (RTES) that were not covered by the standard but are important for COMPLEX objectives.


### 3.1.4 Other Standardization Bodies

Relations and provision of relevant input to other standardisation organisations: e.g. OCP-IP, IEEE DASC, IEEE SA, or other.

OCP-IP related work to IP-XACT is of a special interest for the COMPLEX Project. A Meta-Data WG of OCP-IP is the target working group that can accommodate inputs from COMPLEX. An initial discussion has been carried out between ECSI and OCP-IP (Ian Mackintosh, the OCP President) on the ways of cooperation.
3.2 Interfaces

The following table lists the interface responsible and the different contributors for the transfer of input and interaction between the project and the standardization bodies. The list of standardization bodies is tentative and might be completed with additional organization in future reports.

<table>
<thead>
<tr>
<th>Standardization body</th>
<th>Standard</th>
<th>Interface</th>
<th>Contributors</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACCELLERA</td>
<td>SystemC</td>
<td>Synopsys, ST-I, OFFIS</td>
<td>Synopsys, ST-I, OFFIS</td>
</tr>
<tr>
<td>ACCELLERA</td>
<td>IP-XACT</td>
<td>MDS, ECSI</td>
<td>Synopsys</td>
</tr>
<tr>
<td>OMG</td>
<td>UML/MARTE profile</td>
<td>Thales</td>
<td>GMV, UC</td>
</tr>
<tr>
<td>OCP-IP</td>
<td>OCP</td>
<td>ECSI</td>
<td>MDS, Synopsys</td>
</tr>
</tbody>
</table>

3.3 Contributions

This section includes all the contributions provided to the different standardization bodies.

3.3.1 IEEE P1666

The IEEE working group P1666 worked out the next revision of the IEEE Standard 1666 for the SystemC language [5], released to the general public in September 2011. As voting members of IEEE-SA, SNPS and ST had substantial impact on the approval of new and improved features of SystemC/TLM.

In addition to the proposal of minor enhancements and clarifications, diligent review of proposals, and an active participation in the discussion in the different forums of the P1666 working group, an extended proposal for a new container class `sc_vector` for modules, ports, and other objects had been proposed by OFFIS already in the first period of the project. The proposal has been accepted and further improved during the standardisation process and is included in the final version of the IEEE SystemC standard 1666-2011.

Detailed information, including meeting minutes, proposal details and an archive of the e-mail based discussions during the preparation of the current version of the IEEE 1666 standard can be found on the IEEE P1666 website at [http://www.eda.org/systemc](http://www.eda.org/systemc).

With the release of the revised version of the standard, it is assumed that the activities in the IEEE P1666 working will be quite low in the near future. Initial discussion of potential new features are carried out within the corresponding Accellera Systems Initiative working groups, which act as an incubator before bringing more stabilized solutions back to the IEEE.
3.3.2 Accellera Systems Initiative – SystemC

In addition to the contributions to the IEEE WG P1666, several COMPLEX partners actively contribute to the on-going evolution of the SystemC eco-system within the Accellera Systems Initiative. This includes activities in the relevant Accellera working groups LWG, TLMWG, and CCIWG (formerly OSCI working groups).

3.3.2.1 SystemC/TLM 2.3.0

Alongside with the addition of the \texttt{sc\_vector} class to the SystemC standard, a proof-of-concept implementation has been contributed by OFFIS to the Accellera proof-of-concept implementation of SystemC. Several other proposals from P1666 have been implemented and contributed as well, most notably

- \texttt{sc\_process\_handle} extensions for compatibility with standard C++ containers (OFFIS)
- \texttt{sc\_event\_and/or\_list}, and \texttt{sc\_event\_and/or\_expr} for extended event sensitivity (OFFIS)
- \texttt{sc\_signal} \rightarrow \texttt{sc\_writer\_policy} safely enabling multiple writers (OFFIS)
- virtual \texttt{bind()} methods for ports (OFFIS)
- addition of \texttt{float} support for fixed-point types (SNPS)

The effort in contributing to the proof-of-concept implementation of the SystemC core language has been continued in the current period of the project. The Accellera SystemC LWG has merged the TLM-2.0 implementation into the core package and has released a new version of the proof-of-concept implementation in the middle of 2012 (version 2.3.0). OFFIS has actively contributed fixes and review to this release.

3.3.2.2 Contributions to SystemC LWG/TLM

Within the OSCI LWG, the inclusion of features that have been rejected or not yet considered by the IEEE P1666 WG for the next revision of the SystemC standard (IEEE 1666-2011) are discussed, and COMPLEX partners are actively contributing to resolve the open issues and stabilize these features for industry adoption. The most important challenge in that regard is the extension of the SystemC core language for exploiting multi-core parallelism of the simulator platform. This can lead to an increased simulation performance, which is a core requirement of today’s large-scale virtual platform models, and therefore directly in the scope of the COMPLEX project.

The TLMWG is currently not very active due to the merger of the implementation with the core language. There are discussions within the Accellera Systems Initiative to merge the TLMWG with the core Language Working Group in the near future, since TLM-2.0 is now part of IEEE 1666-2011 and its proof-of-concept implementation is maintained together with the main SystemC kernel.

As part of the non-invasive power augmentation techniques developed in task 2.3, the \texttt{observable sockets} have been developed by OFFIS. These additional convenience sockets \texttt{tlm\_utils::tlm\_observable\_initiator|target\_socket<N>} are expected to be of general interest for various TLM modelling use cases. An initial proposal to submit to the TLMWG has been prepared, but not yet submitted to Accellera, since the current reorganisation within the working groups is not completed, yet. Currently, there are limited
resources available in the related working to discuss new functionality. Any proposal is likely to receive too little attention for a successful adoption.

In March 2013, Philipp A. Hartmann, OFFIS’ technical project manager for COMPLEX, has been nominated as future chair of the SystemC Language Working Group. This nomination has been approved by a unanimous LWG vote in April 2013. Taking over this new role within Accellera, OFFIS’ path towards standardisation of COMPLEX results will be further strengthened in the future.

### 3.3.2.3 Contributions to CCIWG

The current work of the CCIWG (Configuration, Control and Inspection) to define a standardised configuration API is closely followed by the COMPLEX consortium and considered as a future basis for virtual platform configuration. The identified requirements of the COMPLEX framework are reviewed and potential conflicts are communicated back to the CCIWG. Both, Synopsys and OFFIS are actively contributing to the current activities of the CCIWG.

The results of the CCIWG configuration standard are needed as a prerequisite to define a common, standardised model for extra-functional properties in SystemC. As an example, the support for physical units of configuration parameters – which is very important to model physical properties like power – has been discussed under active contribution from COMPLEX partners within the CCIWG.

### 3.3.2.4 Long-term Standardisation

An overall standardised framework for the modelling of extra-functional properties in SystemC will be a long-term goal, since standardisation processes take a lot of time. The COMPLEX results can serve as a significant baseline for a standardisation roadmap in the future.

#### Scalable model for extra-functional properties (power, temperature)

One of the main challenges in that regard will be reaching consensus on an interoperability “Extra-Functional Base Model” (similar to the Base Protocol in TLM-2.0), covering all relevant (power, temperature-related) design parameters in an executable model. Such extra-functional models are highly use-case and methodology dependent. A sketch of such a model is shown in Figure 4, showing the wide variety of possible parameters.

Since such an extra-functional model strongly depends on the parameterisation of a design, it is necessary to postpone a detailed discussion of such a model (parameter names, units, combination rules) after a standardised configuration API (as currently developed in CCIWG) is finalised.

The following requirements should be met for such a power model, as presented to the SystemC community during the keynote talk at ISCUG’2013 (see Section 2.1.9):

- **Simplicity**: Only use those (dynamic) parameters needed for current use case (e.g. ignore area, when not looking for thermal behaviour)
- **Composability**: Derive combined values from physical relations between individual contributors (total power, temperature-dependent power, capacitance-based power)
- **Hierarchy**: Put parameters on “correct” geometric level, inherit parameters from context/environment
• **Adaptivity**: Changing parameters during run-time to support dynamic power management

The standardisation of such an (executable) SystemC power-model should furthermore be aligned with the UPF/CPF related efforts towards ESL power modelling, e.g. by mapping the CPF/UPF concepts to SystemC/TLM simulation model.

![Diagram of a scalable power model](image)

**Figure 4 Example for a scalable power model**

The power model used in COMPLEX follows these paradigms and be used as a baseline for the definition of an interoperability set of parameters combined with rules for composing, using and (run-time) changing of these parameters. The standardisation process of such a detailed model should be postponed after a collection of industry-wide practices and requirements. The on-going standardisation of model configuration (see Section 3.3.2.3) helps with most technical showstoppers already.

**Flexible tracing for extra-functional properties**

SystemC’s built-in tracing capabilities are not sufficient for extra-functional properties, yet. Therefore, another important aspect is the integration of the (power) model parameterisation with a common extra-functional tracing/introspection mechanism, supporting

- hierarchical recording of power information,
- flexible adaptation to granularity of selected power model,
- strongly typed (C++) physical units support, to avoid composition errors.

For this interoperability requirement, the COMPLEX tracing framework, as presented in deliverable D3.1.2 [6] could again serve as a technological baseline, as the above properties are supported already. On the other hand, the CCIWG as natural discussion forum for such mechanisms (related to inspection) needs to finalise the configuration standard first. OFFIS intends to donate the proof-of-concept implementation of the tracing interfaces to Accellera in the future.
3.3.2.5 Short to Medium-term Contributions

Apart from the aforementioned long-term standardization goals for extra-functional modeling in SystemC, two short to medium-term extensions to the core simulation capabilities of SystemC/TLM have been prepared and presented to the SystemC community at ISCUG (see Section 2.1.9) and have been generally well-received. These proposals are not limited to power modeling, but can be used in a variety of use cases. Since both of them are directly related to the core language, their discussion does not depend on the completion of the configuration milestone in the CCIWG, as power model and tracing infrastructure do.

Extended Simulation Callbacks

In order to efficiently integrate the extended tracing mechanisms, a more fine grained control over the simulation (time) advance is needed. While the sc_trace functionality is already internally integrated after the update phase during the simulation, there is no safe state for custom introspection code to extract model information during the simulation.

Especially in TLM-2.0-based virtual platforms with temporal decoupling, transactions may be arriving out-of-order. Since the process scheduling is implementation-defined, it is hard to determine, if all initiators have issued their transactions on a target at a particular time during the simulation. To overcome this limitation, an extended simulation callback mechanism is proposed by OFFIS.

![Extended SystemC simulation cycle (standardisation proposal)](image)

Figure 5 shows the extended simulation cycle with the proposed augmentation of phase callback points. To enable an efficient implementation, callbacks need to be registered explicitly by the designer. A lean proof-of-concept implementation has been developed by OFFIS, as sketched in the following listing:
In addition to the callback interface itself, the proposal includes semantic rules to keep the kernel scheduling stable. This basically covers the allowed event notifications and other language constructs that are allowed from within the callback implementation. The semantic rules have been extended to allow callback subscription to all (also previously existing) simulation phases for maximum consistency. An sc_object may subscribe to multiple phases as well, which may require a discrimination of the current phase via the (already available) sc_get_status function in the callback body.

This extension (and its implementation) will be brought to the SystemC LWG shortly after the end of the COMPLEX project. Initial discussions (around ISCUG as well as with other members of the LWG) have shown a wide interest for such an extension already.

**Extensible TLM Direct Memory Interface**

Another medium-term standardization proposal related to the extension of core language features to enable the integration of accurate extra-functional properties addresses the Direct Memory Interface (DMI) in TLM-2.0.

The TLM-2.0 Direct Memory Interface (DMI) is very useful for high-performance virtual platforms, since it improves simulation speed by enabling memory accesses without sending explicit transactions through the virtual platform (interconnect(s), target). In order to provide a minimum level of timing accuracy, the tlm_dmi class supports explicit timing hints provided by the DMI-allowing components to the DMI-requesting initiator.

On the other hand, the DMI mechanism is very bad for adding explicit extra-functional models to the SystemC platform, because it allows memory accesses without sending explicit transactions through the virtual platform (interconnect(s), target) and therefore prohibits the augmentation of the (architecture) model with extra-functional properties. Adding more hints, like power, to the DMI information would not scale and severely break encapsulation, since the initiator has no knowledge about the internal requirements of DMI-allowing targets.

In order to bridge this gap without disallowing DMI completely, an early extension idea has been proposed by OFFIS: Extensible DMI with optional callbacks attached to the tlm_dmi response. A target (or interconnect) component may indicate the requirement to allow DMI accesses, if, and only if the attached callbacks are triggered by the initiator after the DMI accesses:
The exact API for the callback itself as well as the granularity are not yet decided. Several options may be useful (once per R/W access, once per quantum, both alternatives). After an initial proposal to the TLMWG by OFFIS, the discussion within the working group will hopefully converge on a working solution.

### 3.3.2.6 Other Contributions

Another contribution to the Accellera Systems initiative is the standardization of the SystemC Network Simulation library (SCNSL) to introduce simulation of packet-based networks in SystemC simulation (by EDALab).

### 3.3.3 Accellera – IP-XACT/IEEE1685 Standard

A work has been realized to establish a methodological and technical link between MARTE and IP-XACT.

- MARTE is a standard defined by OMG (Object Management Group) and is based on the UML standard
- IP-XACT is the IEEE 1685 standard defined by ACCELLERA Systems Initiative

The results of COMPLEX in this domain have contributed to the IP-XACT standard through the Extensions Working Group of Accellera where Magillem Design Services is board member.

The technical results delivered by COMPLEX are concerning the semantic alignments between some of the attributes that are common between MARTE and IP-XACT: mainly structural descriptions of components assembly and configuration have been covered. The next figure illustrates the issue to be solved.

Additionally to this work, a methodology has been described to ensure the flow management of IPs and hardware platform description from MARTE to IP-XACT (and then to SystemC.
for instance); the methodology support top down or bottom up approach in order to fulfill industrial user’s needs. With these two elements (semantically alignment and methodology), it is now possible to create so called IP-XACT generators to automate the flow. Magillem has implemented a prototype, but the dissemination through IP-XACT extension working group will allow to other partners to do similar offers. Details of this work and results are available in D2.5.3 and D1.4.1.

### 3.3.4 MARTE standardization (OMG)

As a main standardization activity, UC has prepared a draft of standardization proposal, to be addressed to the MARTE standardization board. The document propose elements included in the COMPLEX profile, and which cover lacks detected for the development of a UML-based model suitable for DSE in an industrial environment.

The elements which up to the current state of the research have been confirmed as lack, and which have been successfully applied in COMPLEX have been selected for the standardization proposal. These include elements for integrating support for design space exploration. This idea follows the contents of the conference presented by Sébastien Gérard (OMG, chief of MARTE standardization group) in FDL 2012, where lacks in design space exploration were recognised. In this conference the work performed in COMPLEX project with respect to that issue was also presented. Additionally ideas for integrating separation of concerns in the UML/MARTE model, regardless of the tool support are also considered in the proposal. Other elements whose need and/or applicability are still under research have been discarded from the proposal draft.

At the time of this report, the document is circulating between UC and GMV, the contributors to the standardization proposal, for final polishing. During the process, contacts are scheduled with Julio Medina, who was member of the core team in the definition of the MARTE standard. Julio Medina is affiliated to the CTR (Real-Time Computing) Department of the University of Cantabria (UC) and keeps close contact with the Microelectronic Engineering Group of the UC, the one involved in COMPLEX project and on the aforementioned proposal.

It is expected that J. Medina feedback helps to polish the proposal and improve the chances for the acceptation of the standardization acceptation.
4 Summary and feedback/effects

The following lists the exploitable results expected from the project and current plans for how these results will be disseminated to benefit the embedded systems development community.

Table 4-1: Dissemination Summary

<table>
<thead>
<tr>
<th>Exploitable Project Result</th>
<th>Dissemination Path Category</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inconsistencies and improvements in the specification of the UML/MARTE profile. IP-XACT improvements SystemC/TLM improvements</td>
<td>Standardization Open Workshops on Standards / Standard Evolutions</td>
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<td>COMPLEX MDA methodology and toolset architecture</td>
<td>Publications and Conferences Exhibition Booths Demos</td>
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<td>Open Workshops Dedicated training sessions Tutorials Demonstration Sessions Conference Booth Presentations</td>
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<td>Open documentation</td>
<td>E-Mailing Project web pages ECSI web page</td>
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</table>
4.1 Feedback/effects

In order to assess the effectiveness of the dissemination activities, the following table lists the most important feedback effects for some of the COMPLEX dissemination activities. The outreach of the COMPLEX website can be found in the Annex of this report.

Please note, that the following feedback effects are not complete, as some details of the resulting contacts and business opportunities – especially for the industrial partners – are confidential in nature.

Table 2 Feedback effects of COMPLEX dissemination activities

<table>
<thead>
<tr>
<th>Dissemination activity</th>
<th>Partner(s) involved</th>
<th>Feedback effects</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISCUG’2013 (see Section 2.1.9)</td>
<td>OFFIS</td>
<td>Several new industrial contacts, interested in future collaboration and access to COMPLEX framework.</td>
</tr>
</tbody>
</table>
| FDL Conferences | ECSI, OFFIS, ALL | • Presentation of results to industry partners (NXP, Bosch, ST, Infineon, …), members of the ESCUG, feedback from the audience received  
• Presentation to Accellera, alignment with the Accellera body on standardization steps |
<p>| FDL 2010 (see Section 2.1.1) | OFFIS | Intensive discussion with colleagues from the german funded SANITAS project (<a href="https://www.edacentrum.de/en/projects/SANITAS">https://www.edacentrum.de/en/projects/SANITAS</a>) where industry partners like Infineon, Bosch and Siemens are involved. A cooperation with another research partner of SANITAS has proofed that a SW timing back-annotation tool can easily be integrated in the COMPLEX flow using the BAC++ API. |
| FDL 2011 (see Section 2.1.2) | OFFIS | Discussion about COMPLEX framework and its integration into industrial verification environments with verification expert from Mentor Graphics. |
| ESCUG 2011 (at FDL 2011) | OFFIS | Presentation and discussion of TLM observable socket idea and proof-of-concept implementation with major industrial SystemC users. |</p>
<table>
<thead>
<tr>
<th>Event</th>
<th>Date</th>
<th>Contact</th>
<th>Details</th>
</tr>
</thead>
</table>
| DATE Conference Booth | Offis, ECSI | ECSI, Offis, ALL | Several valuable contacts with industry representatives:  
  - EDA: Synopsys, Cadence, Mentor, Forte Design, Aldec  
  - Users: ST TR&D, ST UPD divisions, Global Foundries, NXP)  
  - Discussions on COMPLEX approach, feedback collection |
| DATE 2011 (see Section 2.1.4) | Offis | Offis | After exhibition theatre presentation of COMPLEX framework and tools, discussion with big mobile phone manufacturer from China interested in using the framework and tools. |
| DATE 2012 (incl. QVVP’12) (see Section 2.1.3) | Offis | Offis | COMPLEX flyers have been distributed in 1,200 conference bags.  
In depth discussion with Mentor Graphics Virtual Platform expert about their concept of power simulation. Contact to research partner from the HiPEAC NoE interested in power estimation, back-annotation and fast system-level power modelling. Executed one internal follow-up workshop to analyse co-operation possibilities with this research partner. |
| ESLsyn 2011 (see Section 2.1.7) | Offis | Offis | First contact and discussion of the COMPLEX framework idea with research colleagues from USA. |
| ESLsyn 2012 (see Section 2.1.8) | Offis | Offis | Continuation of discussion with US researchers. As follow-up activity a student from Oldenburg has become visiting student at UC of California, Irvine and completed his master thesis on a COMPLEX related topic. |
| Embedded World 2012 & 2013 Workshops (see Section 2.3.9 & 2.3.10) | Offis, ECSI | Offis, ECSI | Discussion about industrial use of the COMPLEX conceptual framework with different external industry partners (Bosch, NXP, Siemens, ST-Ericsson, Infineon, Huawei, Synopsys, Cadence, RealTime Embedded, Motorola, AntMicro, Evatronix,…).  
One follow-up activity with a big manufacturer of telecommunication switches is currently under evaluation/negotiation. |
<table>
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<tr>
<th>Event Type</th>
<th>Audience</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATE Conference</td>
<td>ALL</td>
<td>Large number of partners from industry in the audience: Infineon, Intel, IMC, Thales, NXP, Bosch, Continental, Delphi, EADS Astrium, Selex, … Good technical discussion and exchange of in-depth information</td>
</tr>
<tr>
<td>Co-located Workshops</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Organization of Various</td>
<td>PoliMi</td>
<td>The goal was in larger event to create space where to discuss modeling and design space exploration related problems and to give the possibility to present project results through key-notes (E. Guidetti STM-I, PARMA’11), invited speakers/panelists (P. Hartmann – DEPCP11 and 13) and posters/demo sessions (all the Use Cases and related tools – DEPCP11-13 and RAPIDO 13). The global effect has been in all the events to have started and rised the interest on the project from the scientific community. The feedbacks received and contacts gathered with those type of events were in most of the case from the accademic community. Additionally in DEPCP13 a panel with others EU-project (FP7 and ARTEMIS) have been organized where the scientific and managerial lesson learnt have been shared among the project coordinators.</td>
</tr>
<tr>
<td>Workshop co-located with</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conferences: PARMA 11, DEPCP11-13 and RAPIDO’13 (See Sections 2.3.1, 2.3.2, 2.3.8, 2.3.10, 2.3.11)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| ESLsyn Conferences         | ECSI, OFFIS | Presentation of COMPLEX to the public (mainly outside of Europe):  
  - industry: NEC, Maxim, National Instruments, Cadence, Synopsys, Calypto, Forte Design, Lantiq, DSPlogic, ELDA, Xilinx, Sony, Google, AutoESL, Bluespec, …  
  - academia: UC Berkeley, U Texas, MIT, U Montreal, Ritsumeikan University, NAIST, UC Santa Barbara, UC Irvine, UC LA, Hong Kong Polytechnic University, Tokyo City University, CERN, Virginia Tech, Columbia University, UCSD, Sun Yat-Sen University, … |
<p>| ESLsyn 2012 (see Section 2.1.8) | PoliMi   | After the DSE presentation of PoliMi industrial interest on the framework has been collected from two managers of Cadence and Forte Design and from several members of the academic community. |</p>
<table>
<thead>
<tr>
<th>Event/Occasion</th>
<th>Organization/Tool Suite</th>
<th>Details</th>
</tr>
</thead>
</table>
| March 17, 2011, Exhibition Theatre at DATE / Choosing IP-XACT IEEE 1685 standard as a unified description for timing and power performance estimations in virtual platforms | MDS                     | Following this presentation, we received at Magillem’s booth several kind of interested persons:  
- Academic, to know more and envision possible future collaboration through projects or technical exchanges  
- Industrial from SoC, interested by the management of specifications for virtual platform building with SystemC |
| February 28, 2012, Nuremburg, Germany (at Embedded World) / demos on the IP-XACT tool suite dedicated to virtual platform management | MDS                     | Feed back received at Magillem’s booth: several contacts coming from industrial world, which was new for us as we come from SoC world, have convinced us that our technical positionning was good and promising:  
engineering world is working with specification (some of them in UML) and require a stronger link on virtual platform building (mainly in SystemC) |
| DATE 2013 / Virtual Platform Generation, Integration and Extension of Extra-Functional Properties | MDS                     | Feed back received at COMPLEX’s booth: no a lot, DATE this year was very slow… only academic partners interested by our vision on virtual platform management |
| Accellera – IP-XACT/IEEE1685 Standard                                         | MDS                     | Feed back is positive from partners to leverage on Complex’s result and propose extensions to the standard.                                                                                                                                                     |
| Embedded World 2012                                                           | EDALab                  | Some important industrial contacts for HIFSuite                                                                                                                                                      |
| Embedded World 2013                                                            | EDALab                  | Some important industrial contacts for HIFSuite                                                                                                                                                      |
| Internet http://sourceforge.net/projects/scnsl/                                | EDALab                  | 328 Downloads from Dec. 1st, 2011 (M24 of COMPLEX project) from the following countries:  
1. India  
2. China  
3. United States  
4. Italy  
5. United Arab Emirates  
6. Germany  
7. France |
5 Conclusions

The COMPLEX project results substantially address many of the challenges facing embedded systems developers today in exploiting model-driven development methods and state-of-the-art power and timing estimation techniques in the development of embedded systems, especially in finding the optimal balance between performance and power consumption.

Overall, the pillars that support the dissemination planning for the project are the following:

- Publish the profiles and interfaces used for the COMPLEX tools and technologies to encourage further improvements on current tools or new ones to be developed.
- Submit to standards bodies the extensions developed within the COMPLEX project to existing standards such as MARTE, IP-XACT, SystemC/TLM.
- Make the development tools and training material available using the well-established dissemination channels of the project partners (i.e. project web-page, (potentially) source code repository).

These coupled with the publication of technical papers and presentations at various conferences allowed to ensure the visibility and awareness of COMPLEX results to a wide range of industrial and academic organizations in Europe and world-wide for the use and exploitation according to their own needs and benefits.

The COMPLEX project applied all possible existing means and dissemination channels to inform the community of the project achievements. Beyond that, COMPLEX created new events that have ambition to inform and educate the engineers and scientists and contribute to advances of advanced design technology. The examples of ESLsyn Conference or the Workshop on Virtual Platforms at Embedded World Conference show that there is a large interest and need to continue these efforts.
6 References


Annex

Google analytics website access statistics for http://complex.offis.de:

5,739 people visited this site

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