Automatic Abstraction of RTL IPs into Equivalent TLM Descriptions for Platform Simulation

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Outline

• HIFSuite overview
• Motivation for abstraction
• Abstraction techniques
• Tool features
• Tested benchmarks
HIFSuite overview
HIFSuite overview

RTL to TLM abstraction tool

HIF core-language

HIF APIs

Manipulation tools

H2H: front-end conversion tools

H2H: back-end conversion tools

VHDL

Verilog

SystemC RTL

SystemC TLM

VHDL

Verilog

SystemC RTL

SystemC TLM

NuSMV
Why automatic abstraction?
Why automatic abstraction?

- RTL simulation is slow
- Is the transactor correct?
Why automatic abstraction?

- Fast simulation
- Correct by construction
- OSCI TLM 2.0 compliant

Untimed/Loosely Timed
- Quantum Keeper (QK)
- Delay Time (DT)
  DT=0 if Untimed

Approximately Timed
- Delay Time (DT)
- 2-4 phases
Merge of states and clk abstraction

RTL

A

B

TLM

A'

ef_0

uf_0; uf_1;

uf_2;

clk & ef_0

clk & ef_1

clk & ~ef_1

while (\sim ef_1) { 
  uf_2 
} 
uf_1;
Tool features

• Merge of states and clock abstraction
• RTL communication protocol abstraction
• Cycle accurate to transaction accurate behavior abstraction
• Correct-by-construction TLM IPs
  – event based equivalence
• 10x to 100x speedup depending on
  – RTL IP structure and target TLM protocol
Tested benchmarks

• Div, Dist, Root  
  – Face Recognition System by STMicroelectronics  
  VHDL/SystemC-RTL

• ECC, CRC  
  – VERTIGO project Platform by STMicroelectronics  
  VHDL/SystemC-RTL

• Bxx  
  – ITC-99 suite  
  VHDL/verilog

• ADPCM  
  – Opencore  
  SystemC-RTL

• FFT  
  – Magali Platform by CEA-Leti  
  VHDL

• I2C  
  – COMPLEX project platform by STMicroelectronics  
  VHDL
The tool
Thank you

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